

**GAFE7 Design Review Material
SLAC.OM.03MAY20**

**This PDF file describes the GAFE7.
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GAFE Specification Summary

SLAC.OM.16MAY03A

Level 4					LAT-SS-00352-01-D7		GAFE7 Simulation Result			Unit
	Min	Nom	Max	Unit	GSFC-663-ACD-000 Draft 3	VCC=3.3+/-10% -20C<T<60C	Min	Nom	Max	Unit
5.2		0.3		MIP	Detection Threshold			0.3		MIP
5.3	0.1	0.3	2	MIP	Veto Threshold Range		0		6	MIP
		0.05		MIP	Veto Adjust Step Size				0.01	MIP
5.4			10	kHz	System False Trigger Rate @ Ttrig=0.15MIP			0.004		MIP eq. Noise
5.5	20		64	MIP	High Range Threshold		0		70	MIP
5.8.1	<u>50</u>		700	ns	Veto Latency			50	200	ns
5.8.2	<u>300</u>		1200	ns	Veto Width up 1 MIP				1000	ns
	<u>300</u>		10000	ns	Veto Width up to 1000 MIP's				5000	ns
5.8.3			50	ns	Veto Recovery after end of Veto				50	ns
5.9.3			0.02, 5%	MIP	Pulse Height Precision to 10 MIP's				0.01	MIP eq noise,
			1.0, 2%		Pulse Height Precision 10 - 200 MIP's				1	MIP eq noise,
5.9.4			18.5	us	Pulse Height Latency		3	3.5	4	us
5.9.5			2%		Integral Non Linearity				1%,25%,50%	full scale
5.9.6			1/2048	full scale	Differential Nonlinearity				1/4096,2/4096,4/4096	full scale
5.9.7			500	ppm/C	Temperature Stability of Gain				100	ppm/C
			0.05	%/C	Temperature Stability of Baseline				0.01	%/C
5.20.2			3	kHz	Input Pulse Frequency				5	kHz
5.2.2.2		640		fC/MIP	PMT Gain			640		fC/MIP
Other	Min	Nom	Max	Unit	SLAC					Unit
Ivcc	0.6	1.4	2.2	mA			1	1.5	2	mA
Ivdd	0.6	0.8	1	mA			0.6	0.8	1	mA
Vcc	2.97	3.3	3.63	V			2.97	3.3	3.63	V
Vdd	2.97	3.3	3.63	V			2.97	3.3	3.63	V
Temp	-20	20	60	c	dT	80	-20	20	60	c
Pulse Height Baseline Span							1.9		2.4	V
Pulse Height Gain								314		mV/pC
Calibration							0		1K	MIP
Autorange Threshold, Output Referred							100		200	mV at MuxSH
Autorange Threshold, Input Referred								9.75		MIP

Underlined specs depend on the digital veto pulse stretching circuitry in the GARC

GAFE7 Modifications

GAFE7 corrects operation for full temperature and power specifications, and lowers the gain per GAFE5 Test Results.

SLAC.OM.16May03v1

GAFE5 Cell	GAFE7 Cell	Concern	Essential	Modification
logo_gafe5f	logo_gafe7a			Low VCC Bias circuit , Gain Range Crossover, Veto Stability, HLD DAC Span adjustments
gafe5f_lvs	gafe7a_lvs	Low VCC operation	yes	Subcell Update
buf1.1	buf1_7.1	Low VCC operation	yes	modified bias, adjusted fet sizes and compensation for power consumption and loading
buf1.1	bufd1_7.1	Low VCC operation	yes	modified bias, adjusted fet sizes and compensation for power consumption and loading
cmp1.1	cmp1_7.1	Low VCC operation	yes	modified bias, adjusted fet sizes and compensation for power consumption and loading
gafe_5fsim.1	gafe_7asim.1			Subcell Update
gafe_v5f.1	gafe_v7a.1			Subcell Update
hamp5c.1	hamp7.1	Gain Adjust, HLD Range		Subcell Update, raised HLD maximum threshold
hold1.1	hold1_7.1			Subcell Update
oalog5f.1	oalog7a.1			Subcell Update
obuffers5f.1	obuffers7a.1	Low VCC operation		increased gain to 1.5
odac35c.1	odac3_7.1	Gain Adjust		Lowered Baseline, Updated Buffers
odacr15d.1	odacr1_7.1	Gain Adjust		Adjusted Range Crossover Threshold and PH Baseline, New Buffer
odacs5d.1	odacs7.1			Subcell Update
odiscs.1	odiscs_7.1	Veto Recovery		added clamping FET to the veto preamplifier feedback, updated Veto discriminator to type rcvrf
odpads.1	odpads7.1			Separated VDD's for simulation analysis
olvsrx.1	olvsrx7.1			Subcell Update
opa1.1	opa1_7.1	Low VCC operation	yes	modified bias, adjusted fet sizes and compensation for power consumption and loading
opa2.1	opa2_7.1	Low VCC operation	yes	modified bias, adjusted fet sizes and compensation for power consumption and loading
opa2b.1	opa2b_7.1	Low VCC operation	yes	modified bias, adjusted fet sizes and compensation for power consumption and loading
opap1f.1	opap1f7.1	Low VCC operation	yes	modified bias, adjusted fet sizes and compensation for power consumption and loading
opha.1	opha7.1	Low VCC operation	yes	modified bias, adjusted fet sizes and compensation for power consumption and loading
orcvrfe.1	orcvrfe7.1	Low VCC operation	yes	modified bias
orxdr.1	orxdr7.1			Subcell Update
osarg1.1	osarg7.1	Gain Adjust		adjusted first and third stage gains
pres.1	pres7.1	Veto Recovery		decreased bias current
rbk2.1	rbk2_7.1			no change, could use old symbol

SLAC.OM.10Dec02v1

GAFE3 was intended to stabilize the GAFE analog circuits.

GAFE4 added AC coupling and finer adjustment steps to the Veto discriminator, as well as a high range charge injection mode, and more crosstalk reduction in the DAC, fe gain reduced to meet the spec of 10us veto recovery from 1000 to 0.1 MIP
The remaining spec not met is the high energy pulse height linearity.

GAFE3 Modifications

subcells in reference to schematic and layout names:

logo	gafe3
corer	new logic for oe polarity
opa2	modified topology for frequency compensation and low side compliance
opa2b	modified topology for frequency compensation and low side compliance
opap1	modified topology for frequency compensation
rbk2	raised threshold to 0.75v per low side compliance uncertainty
buffers	replaced with buffer from GCFE7 for increased slew rate
digdvs	added enable gates for LLD and CHID
dacs	added 3 more opa2s for VBSA isolation
rxdr	removed LLD pad driver

GAFE3 Errata

Low yield due to dc offsets and veto span requirements
Possible increased veto recovery time due to dac coupled crosstalk
High energy range pulse height gain changes 10% over signal range
Slow LVDS receivers due to unintended compensation added to opap1

GAFE4 Modifications

alog	added ports for vdc bias distribution
discs	ac coupled veto discriminator, new auto discriminator has more compliance
test	add high energy cal inject
dacs	added 3 opa2s for VDC isolation, modified dac2 to veto vernier
apads	annotated resistor in pad2det
dpads	adjusted count for LVS
otpads	test points for bias filtering
digdvs	disabled LLD path
corer	used mode2 for high energy cal enable
rbk2	lower threshold to 0.4v , approx. 8 MIP autorange crossover
sarg1	lower fe gain from 16 to 20pF
dact	removed buffer amp to improve low signal calibration
dacs	add resistor to derive vref from vdd

GAFE4 Errata

Double use of mode 2 bit (0=autorange on, hical off, 1=autorange off, hical on)
Logo says GAFE3
Autorange crossover may be a bit low and temp sensitive (ie 8+/- 1 MIP vs temp)
Preset values are not optimal due to gain and bias changes.
Reg 6 still readbacks version 3 since core did not change.
The remaining spec not met is the high energy pulse height linearity.

GAFE5 Modifications

ocore5	brought out reg 0 bit 6
opadbidir2	enlarged bond pad, and back annotated pad capacitance
odpads2	instanced new padbidir
gafe_v5	replaced mode2 with mode6 to gate hi level cal pulse, new dpads
logo	added gafe5b logo

GAFE5 Errata

n71a is a Level 3 Model, expected operating point obtained at 3.6vcc.
t12l fit test results to about 20%

GAFE 4 Results GAFE 5 Results

GAFE Parameter	voltage 3.3	voltage 3.4	voltage 3.6	voltage 3.3	voltage 3.4	voltage 3.6		Units
Analog Current	1.01	1.08	1.48			1.49		mA
Digital Current	0.86	0.91	1.02			1.05		mA
Read/Write Regs	OK	OK	OK			OK		
BIAS DAC GAIN LE	-116.4	-116.5	-116.6			-111		ADUs/step
BIAS DAC OFFSET LE	324.8	338.7	364.6			602		ADUs
BIAS DAC GAIN HE						-110		ADUs/step
BIAS DAC OFFSET HE	50.4	62.1	91.1			992		ADUs
BIAS DAC 0 Volts LE	2.302	2.291	2.273			2.118		volts
BIAS DAC 7 Volts LE	2.814	2.805	2.788			2.61		volts
BIAS DAC 0 Volts HE	2.479	2.459	2.442			1.893		volts
BIAS DAC 7 Volts HE	2.991	2.979	2.967			2.369		volts
Peak Hold Delay CMD	30	28	27			36		50 nsec
PHA Gain LE	676.8	681.5	689.4			690		ADUs/pC
PHA Offset LE	324.6	341.8	371.4			176		ADUs
PHA Range LE	3.8	4.9	5.1			5.7		pC
PHA Noise LE	4.5	4.5	4.4			5		ADUs
PHA INL LE						5		ADUs
PHA Gain HE	7.54	7.38	7.27			7.45		ADUs/pC
PHA Offset HE	31.2	48.4	83.7			559		ADUs
PHA Range HE	250	330	500			300		pC
PHA Noise HE	3.5	3.5	4			3		ADUs
PHA INL HE						10		ADUs
Crossover Charge	4.2	4	3.9			5.5		pC
Crossover PHA	3100	3100	3100			3900		ADUs
DNL LE								
DNL HE								
Veto DAC 0.2	59	59	59			60		cmd
Vernier DAC 0.2	36	34	32			7		cmd
HM Delay CMD	9	10	11			10		50 ns
Veto DAC 0 Thresh	7.5	6.9	6.2			6.7		pC
Veto DAC 56 Thresh	0.7	0.52	0.6			0.6		pC
Veto DAC Step Size	-0.121	-0.114	-0.100			-0.109		pC/step
Vernier DAC 0 Thresh	0.64	0.615	0.58			0.63		pC
Vernier DAC 63 Thresh	0.42	0.41	0.39			0.425		pC
Vernier DAC Step Size	-3.93	-3.66	-3.39			-3.66		mpC/step
HLD 59 Threshold	1.9	1.9	1.9			2.8		pC
HLD 55 Threshold	11.1	11.2	11.3			6.7		pC
HLD 45 Threshold	32.8	33.5	33.9			16.3		pC
HLD 35 Threshold	53.5	55.1	56.5			25.7		pC
HLD 25 Threshold	72.8	76	78.7			35.1		pC
HLD 15 Threshold	90.3	95				44.5		pC
HLD DAC Step Size	-2.01	-2.12	-1.79			-0.95		pC/step
HLD DAC Offset	122.47	128.4	135.3			59		pC
Veto, HLD EN Cmd Bits	OK	OK	OK			OK		
TCI Reg Range Gain	91.75	91.8	92.81			93		ADUs/step
TCI Reg Range Offset	336.2	353	384.68			179		ADUs
TCI Reg Range Range	24	24	24			24		steps
TCI Reg Range Noise	5.4	5.4	5			5		ADUs
TCI High Range Gain	18.45	18.75	19.06			17.6		ADUs/step
TCI High Range Offset	51.75	63.75	94.84			553		ADUs
TCI High Range Range	24	24	24			24		steps
TCI High Range Noise	2.3	2.2	2.1			2		ADUs

GAFE5 Power Consumption and Gain Measurement and Simulation Comparison

OM 6MAY03

v3

http://www.slac.stanford.edu/~milgrome/gafe5_debug/gafe5_su3_Test_vs_Simulation.pdf

DUT: GAFE5#3

Room Temperature

VCC=3.60V

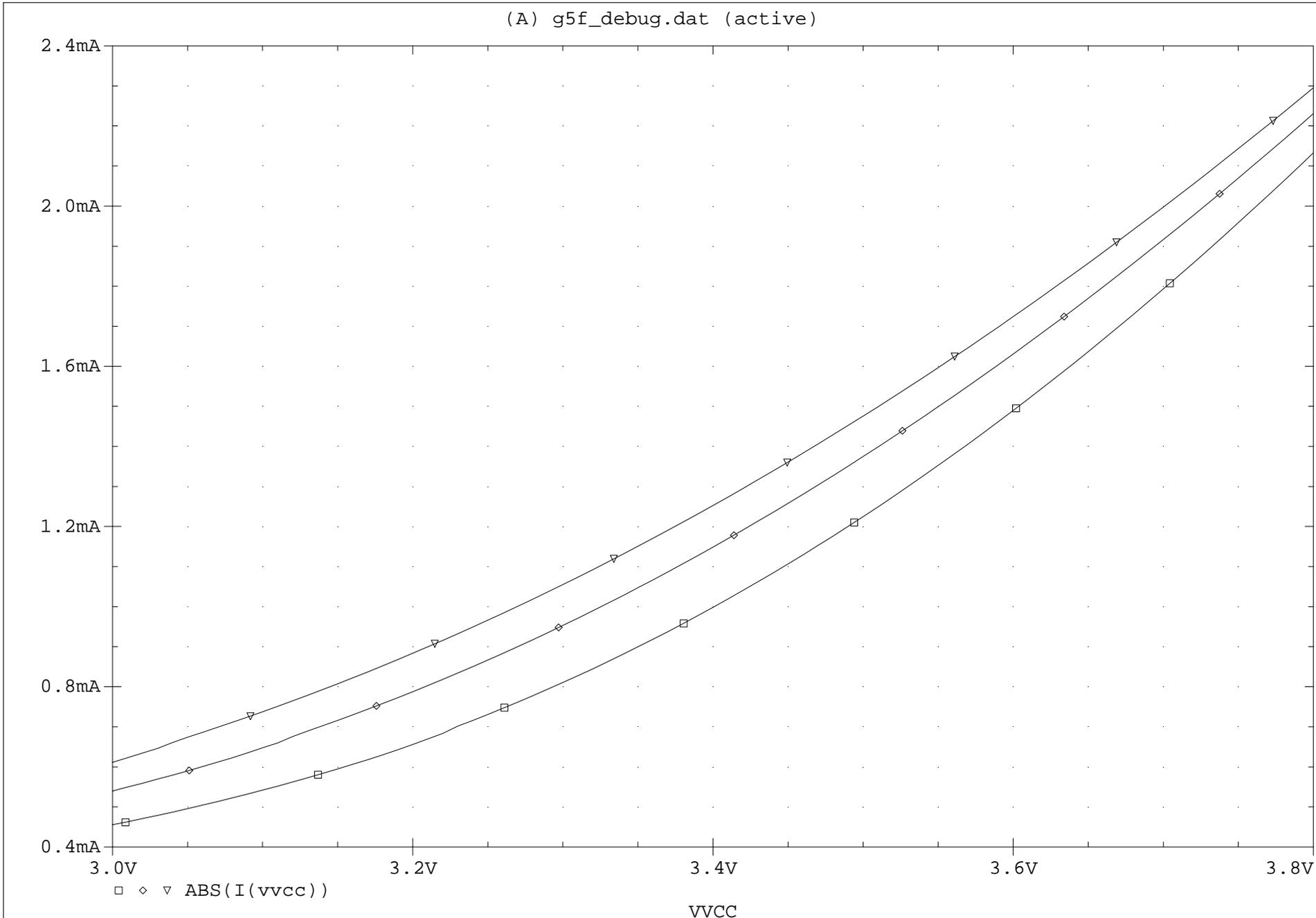
Page

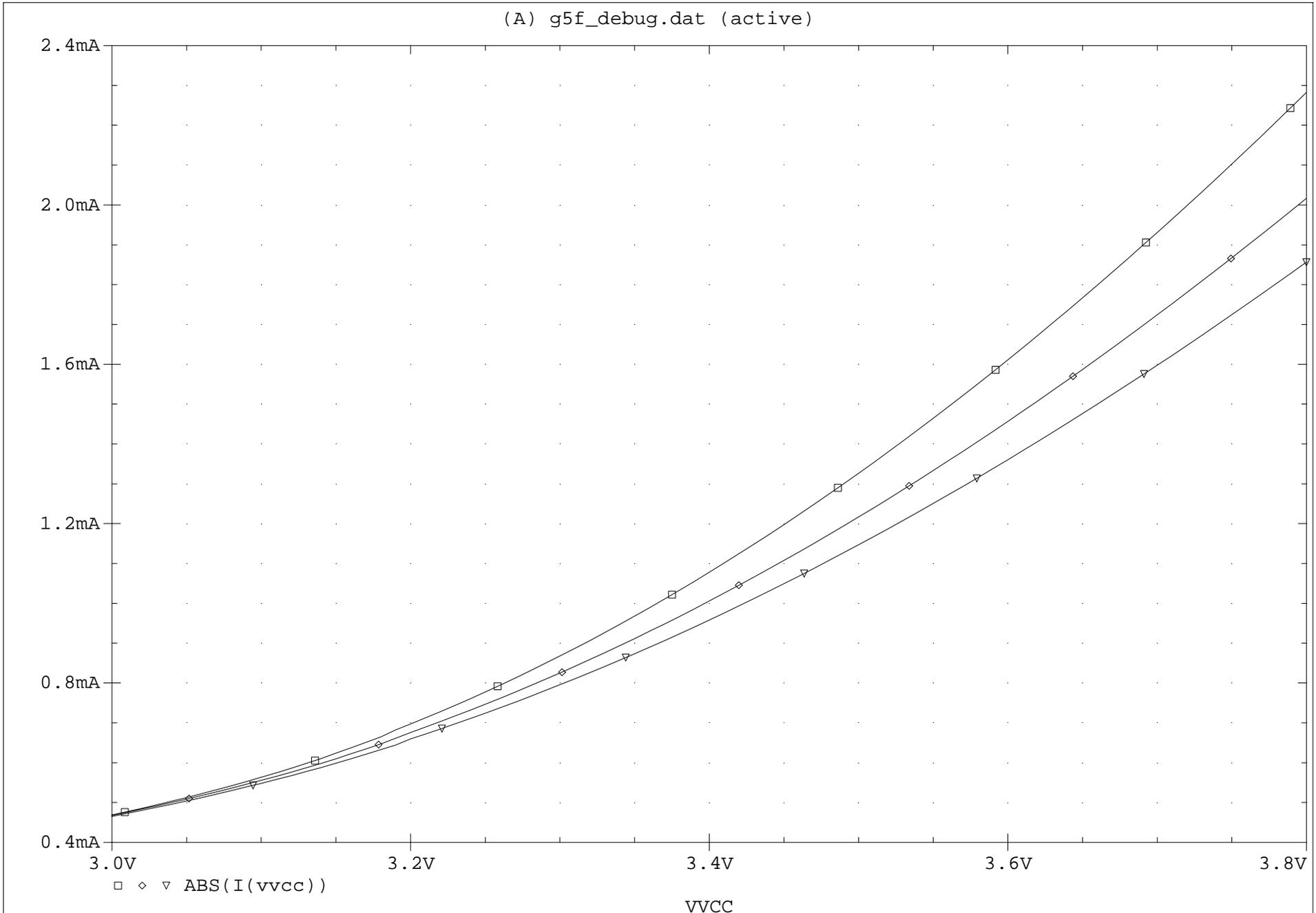
1) ICC vs VCC, Measured vs Simulations

Test Data: SU3							Simulated:			
VCC, VDD	ICC_test	IDD_test	GSFC IVCC	GSFC IVDD	% Error to SU3		ICC_N84A	% Error to SU3	ICC_T12L	% Error to SU3
Volts	mA	mA	mA	mA	IVCC	IVDD	mA		mA	
3.80	1.81	1.13					2.23	23.20	2.02	11.60
3.60	1.36	1.01	1.48	1.02	8.82	0.99	1.63	19.85	1.45	6.62
3.50	1.21	0.96					1.38	14.05	1.22	0.83
3.40	0.97	0.92	1.08	0.91	11.34	-1.09	1.15	18.56	1.01	4.12
3.30	0.85	0.86	1.01	0.86	18.82	0.00	0.95	11.76	0.83	-2.35
3.00	0.55	0.73					0.55	0.00	0.48	-12.73

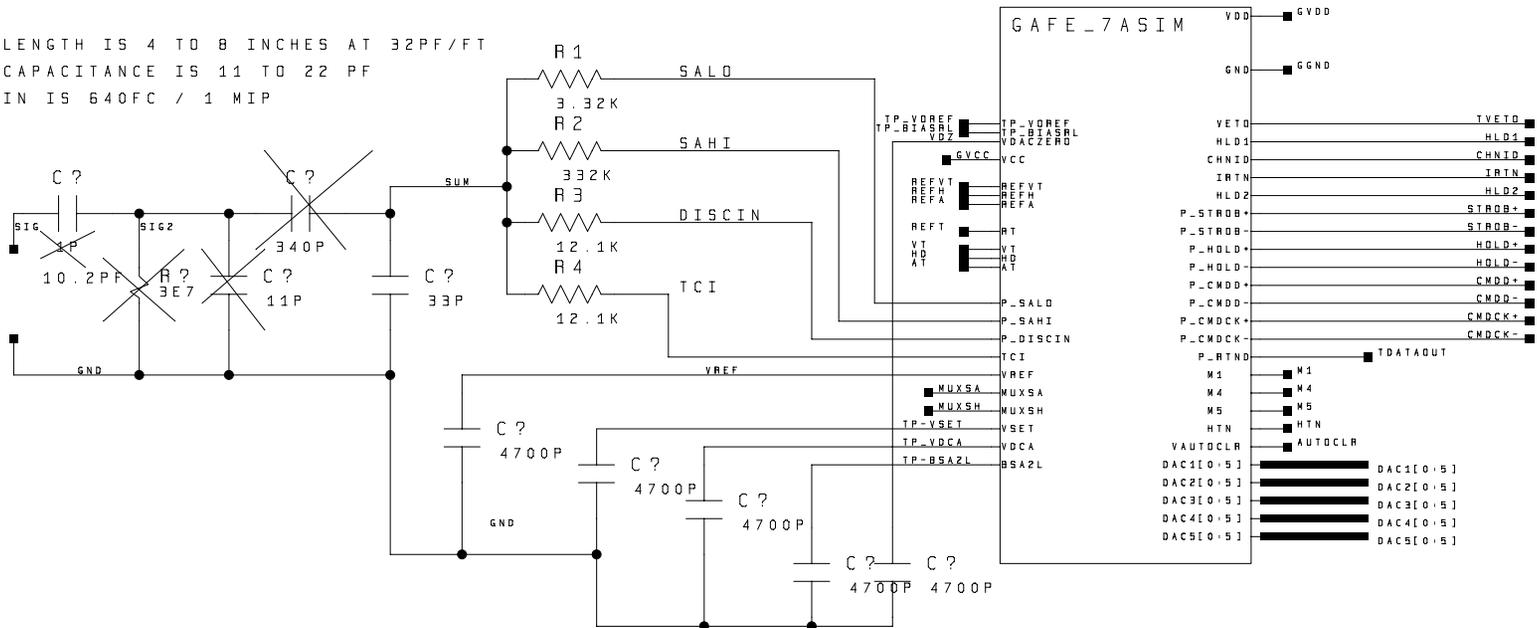
As explained on page 11, N84A is the BSIM model set from MOSIS which was fit over temperature. T12L is the SLAC reference library from the MOSIS T12L run BSIM room temp fit.

- 2) Plot of ICC vs VCC and temperature using model set N84A
- 3) Plot of ICC vs VCC and temperature using model set T12L
- 4) Schematic of the Test Bench changes required to fit data: the PMT model was replaced with a 10.2pF voltage pulser.
- 5) Scope plot of 1pC response (1.56MIP) GAFE5_S3 High Gain 440.00 mV/pC
GSFC 421.00 mV/pC -4.32
- 6) Simulation of 1pC response N84A High Gain 420.00 mV/pC -4.55
- 7) Scope plot of 10pC response GAFE5_S3 Low Gain 5.04 mV/pC
GSFC 4.50 mV/pC -10.71
- 8) Simulation of 10pC response N84A Low Gain 4.61 mV/pC -8.53
- 9) Scope plot of 100pC response GAFE5_S3 Low Gain 0.61 mV/pC
- 10) Simulation of 100pC response N84A Low Gain 0.52 mV/pC -14.75
- 11) Excerpt from the MOSIS Spice Model FAQ explaining the BSIM temperature limitations
- 12) More from the MOSIS Spice Model FAQ explaining their BSIM model accuracy
- 13-15) Test Bench Stimuli Bias DAC 3 Veto DAC 60.45 simulated 57.00 tested





CABLE LENGTH IS 4 TO 8 INCHES AT 32PF/FT
 CABLE CAPACITANCE IS 11 TO 22 PF
 PMT GAIN IS 640FC / 1 MIP



STANFORD LINEAR ACCELERATOR CENTER

4-29-2003_15:56

CALIBRATION_SIM_

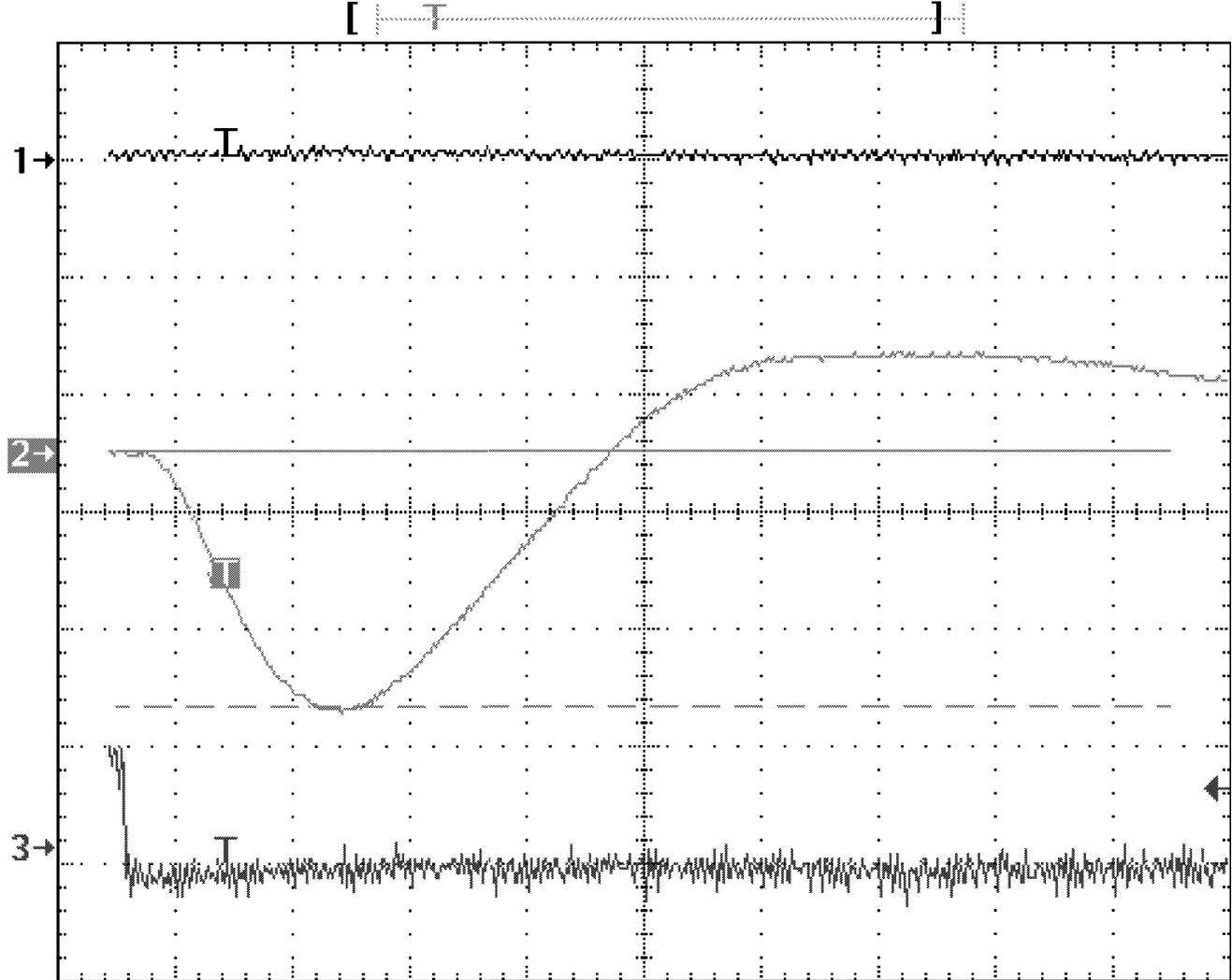
LHEA - NASA

DRAWN BY:

D

Tek **Stop:** 25.0MS/s

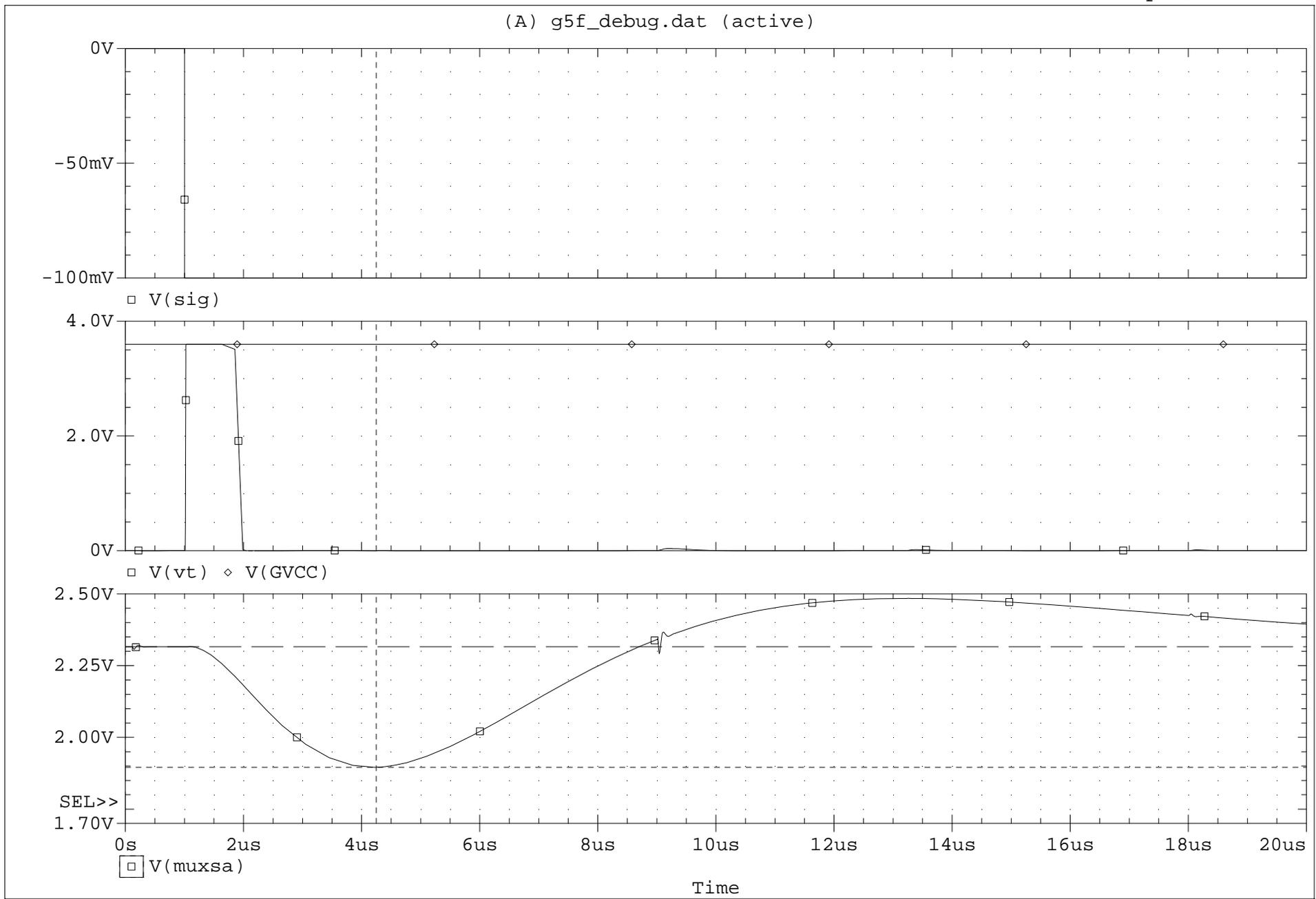
53 Acqs



Δ : 440mV
@: 4mV

Ch1 500mV \wedge Ch2 200mV \wedge B_w M 2.00 μ s Ch3 ∇ 48mV
Ch3 100mV

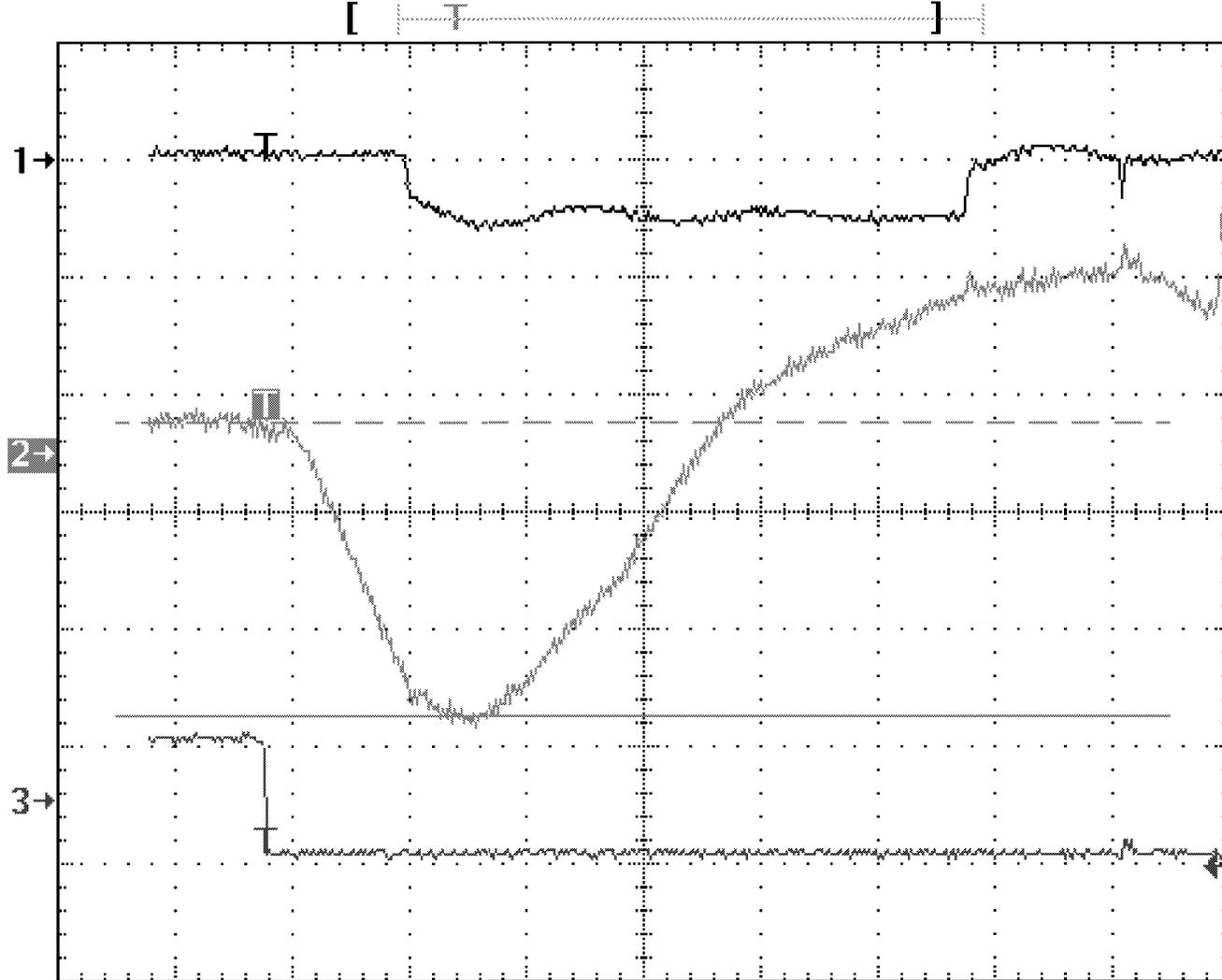
6 May 2003
17:48:52



A1:(4.2472u,1.8958) A2:(0.000,2.3161) DIFF(A):(4.2472u,-420.249m)

Tek **Stop:** 25.0MS/s

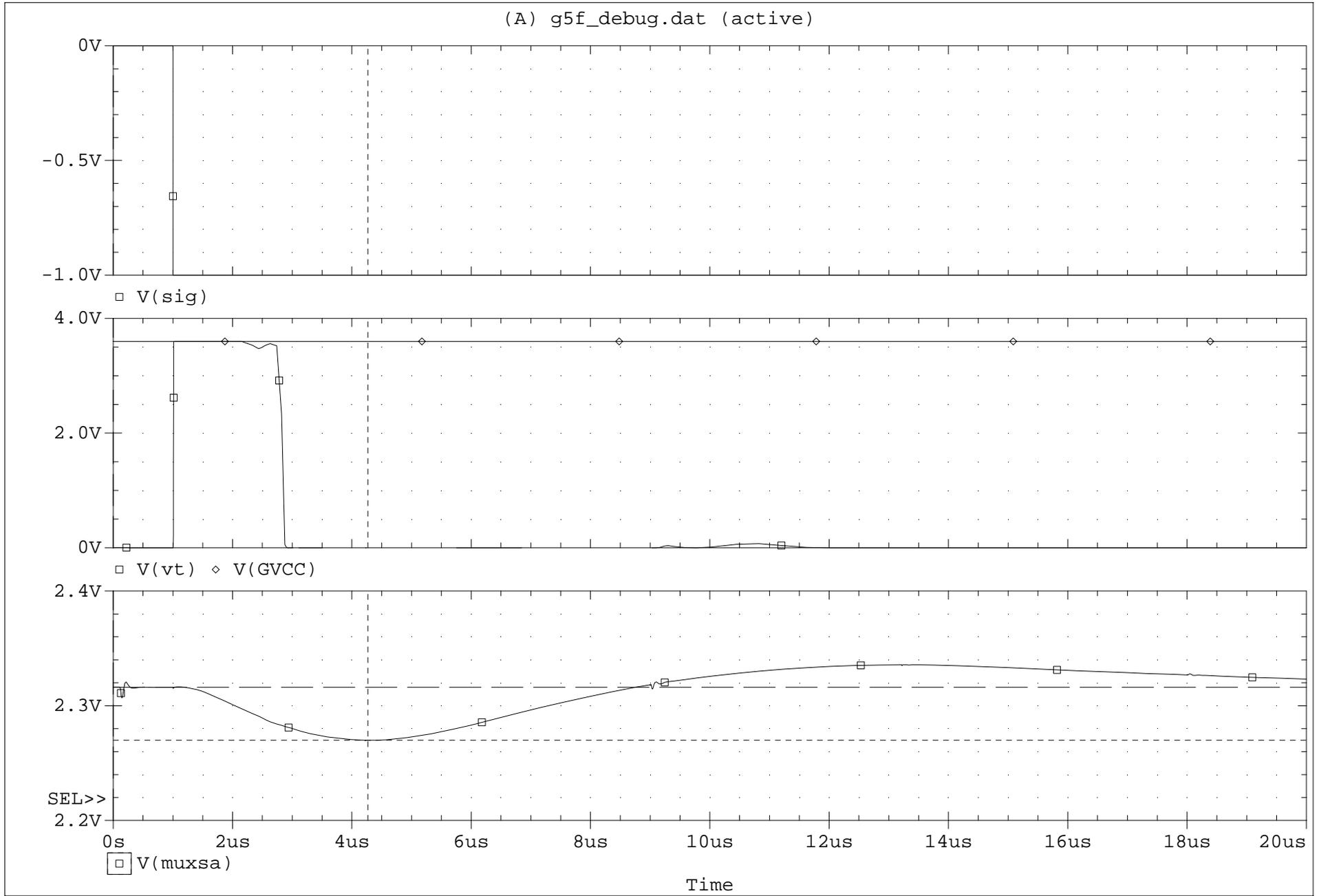
13 Acqs



Δ : 50.4mV
@: -45.2mV

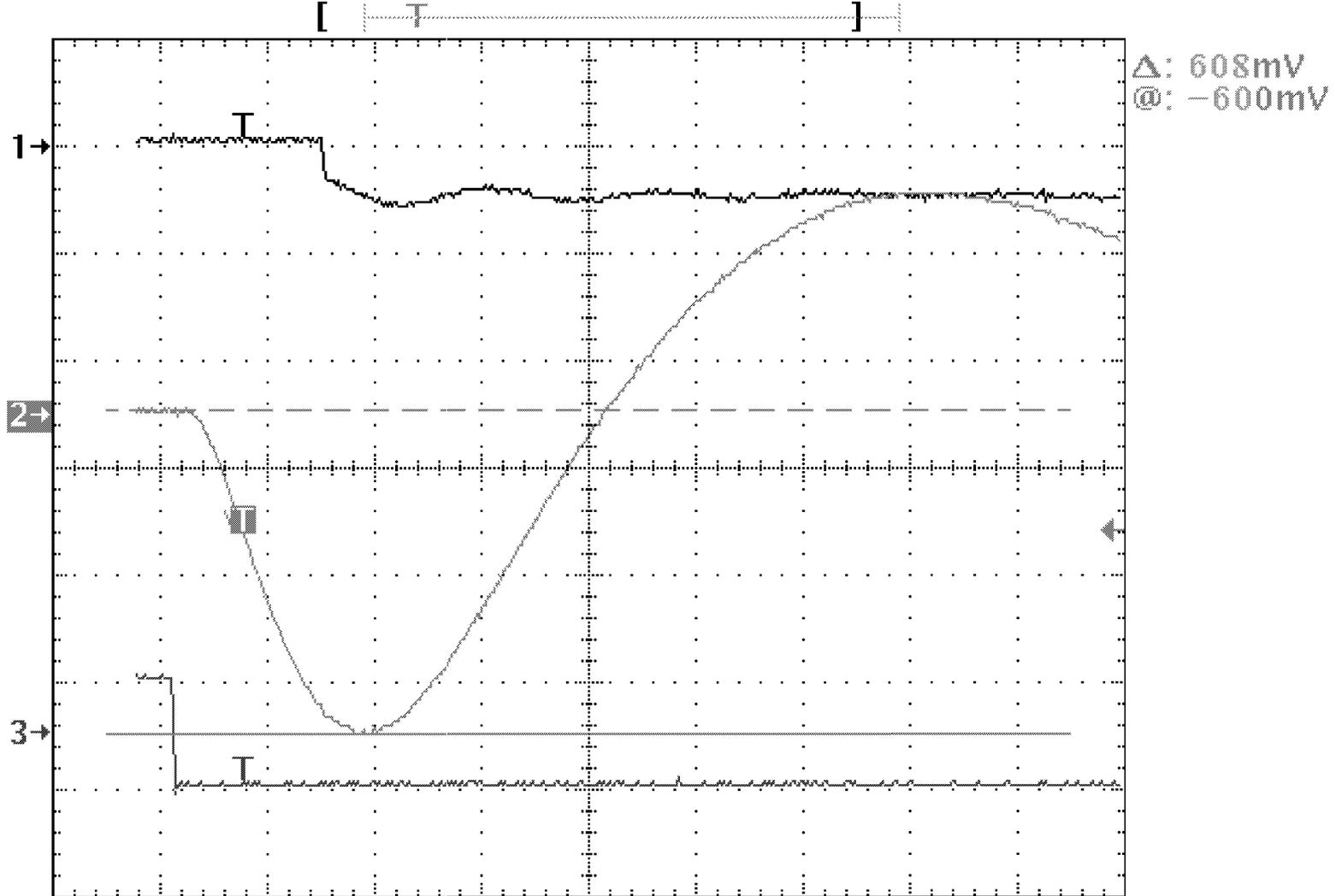
Ch1 500mV/V Ch2 20.0mV/V M 2.00 μ s Ch3 \sim -580mV
Ch3 1.00 V

6 May 2003
17:43:28



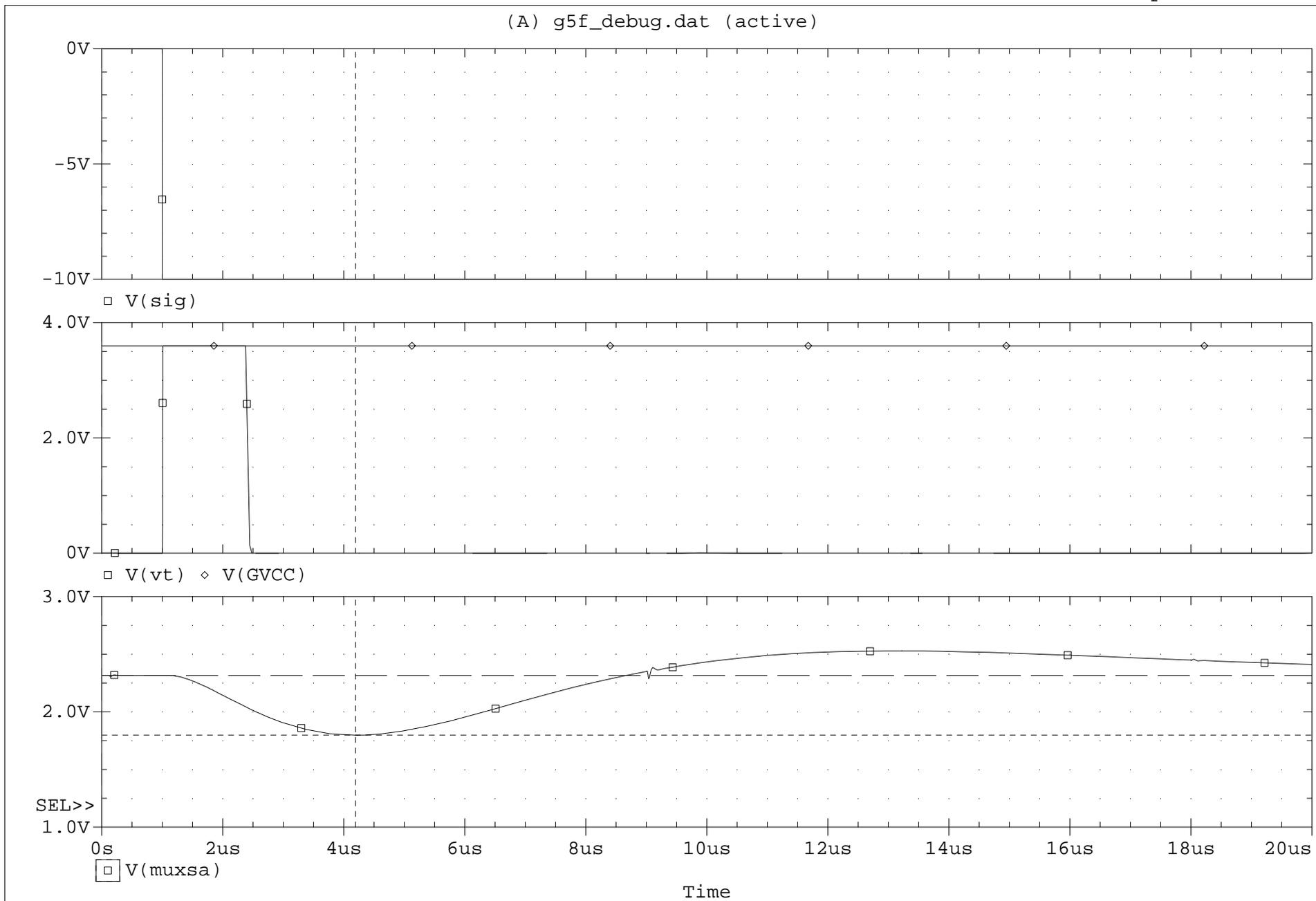
A1: (4.2667u, 2.2699) A2: (0.000, 2.3161) DIFF(A): (4.2667u, -46.167m)

Tek Run: 25.0MS/s Sample



Δ: 608mV
@: -600mV

Ch1 500mV
Ch3 10.0 V
Ch2 200mV M 2.00μs Ch2 -220mV 6 May 2003 17:41:05



A1:(4.1978u,1.7979) A2:(0.000,2.3161) DIFF(A):(4.1978u,-518.121m)

```

                                g5f_debug.cir
GAFE5F DEBUG SLAC.OM BSIM CALIBRATION T=20C N84A.mod VCC=3.6V
* .op
* .dc VVCC 3 3.8 .01
.param vccc=3.6
.option nomod
.tran ln 20u
rconverge sum tp_vdca le9
* .savebias "5f_bias7.txt" tran time=ln
.loadbias "5f_bias6.txt"
.param vmult=1
.param vpk=-.1
.param cdz=1f
.param ctest=10.2p
.probe v([N1I293NC_CS]) v([autoclr]) v(943) v(945) v(953) v(951) v(947)
.probe v([N1I293UI_REG_CH]) v(941) v(944) v(946) v(940) v(942)
.probe v([sig]) v([sig2]) v([sum]) v([salo]) v([sahi]) v([discin]) v([tcil]) v([vref])
.probe v([muxsa]) v([muxsh]) v([tp-vset]) v([tp_vdca]) v([tp-bsa21])
.probe v([tveto]) v([chnid]) v([tdataout])
.probe v([refvt]) v([refh]) v([refa]) v([n1i293dcb]) v([n1i293dcc]) v([n1i293dcd]) v([r
eft]) v([strob+]) v([hold+])
.probe v([N1I293CS]) v([N1I293ADO]) v([N1I293HLD]) v([N1I293SI])
.probe v([vt]) v([hd]) v([at]) v([N1I2931I293ALO]) v([TP_VOREF]) v([GVCC])
.probe i(vvdd) i(vvee) i(vsub) i(vvcc)
.option opts
.option itl1=1500
.option itl2=200
.option itl4=100
.option defad=1e-10
.option defas=1e-10
vref vref 0 2.5
vpmt sig 0 0
+ pwl (
+ 0 0 1u 0
+ 1.001u {vmult*vpk} 30u {vmult*vpk}
+ 30.001u {vmult*(vpk+vpk)} 40u {vmult*(vpk+vpk)}
+ )
* these gozinta
* autorange clear-bar

```

```

                                g5f_debug.cir
VAUTOCLR AUTOCLR 0 0
+ PWL (0 0 10n 0 11n {vccc})
* dacs = vtm60 vvm44 hd32 bl3 cal63
* veto trim best is 333300 60h
* best is 333300
VDAC10 DAC10 0 0
*+ pulse ( 0 3 1u 10n 10n 1u 2u)
VDAC11 DAC11 0 0
*+ pulse ( 0 3 1u 10n 10n 2u 4u)
VDAC12 DAC12 0 3
*+ pulse ( 0 3 1u 10n 10n 4u 8u)
VDAC13 DAC13 0 3
*+ pulse ( 0 3 1u 10n 10n 8u 16u)
VDAC14 DAC14 0 3
*+ pulse ( 0 3 1u 10n 10n 16u 32u)
VDAC15 DAC15 0 3
*+ pulse ( 0 3 1u 10n 10n 32u 64u)
* veto trim best is 303300 44 or 45
VDAC20 DAC20 0 3
*+ pulse ( 0 3 1u 10n 10n 10u 20u)
VDAC21 DAC21 0 0
*+ pulse ( 0 3 1u 10n 10n 20u 40u)
VDAC22 DAC22 0 3
*+ pulse ( 0 3 1u 10n 10n 40u 80u)
VDAC23 DAC23 0 3
*+ pulse ( 0 3 1u 10n 10n 80u 160u)
VDAC24 DAC24 0 0
*+ pulse ( 0 3 1u 10n 10n 160u 320u)
VDAC25 DAC25 0 3
*+ pulse ( 0 3 1u 10n 10n 320u 640u)
* hld nominal dac3 is 32, preset=
VDAC30 DAC30 0 0
*+ pulse ( 0 3 1u 10n 10n 1u 2u)
VDAC31 DAC31 0 0
*+ pulse ( 0 3 1u 10n 10n 2u 4u)
VDAC32 DAC32 0 0
*+ pulse ( 0 3 1u 10n 10n 4u 8u)
VDAC33 DAC33 0 0

```

g5f_debug.cir

```

*+ pulse ( 0 3 1u 10n 10n 8u 16u)
VDAC34 DAC34 0 0
*+ pulse ( 0 3 1u 10n 10n 16u 32u)
VDAC35 DAC35 0 3
*+ pulse ( 0 3 1u 10n 10n 32u 64u)
* baseline nominal dac4 is 3, preset=
VDAC40 DAC40 0 3
*+ pulse ( 0 3 1u 10n 10n 1u 2u)
VDAC41 DAC41 0 3
*+ pulse ( 0 3 1u 10n 10n 2u 4u)
VDAC42 DAC42 0 0
*+ pulse ( 0 3 1u 10n 10n 4u 8u)
*VDAC43 DAC43 0 0
*+ pulse ( 0 3 1u 10n 10n 8u 16u)
*VDAC44 DAC44 0 3
*+ pulse ( 0 3 1u 10n 10n 16u 32u)
*VDAC45 DAC45 0 3
*+ pulse ( 0 3 1u 10n 10n 32u 64u)
* cal nominal dac5 is 63, preset=
VDAC50 DAC50 0 0
*+ pulse ( 0 3 1u 10n 10n 1u 2u)
VDAC51 DAC51 0 0
*+ pulse ( 0 3 1u 10n 10n 2u 4u)
VDAC52 DAC52 0 0
*+ pulse ( 0 3 1u 10n 10n 4u 8u)
VDAC53 DAC53 0 0
*+ pulse ( 0 3 1u 10n 10n 8u 16u)
VDAC54 DAC54 0 3
*+ pulse ( 0 3 1u 10n 10n 16u 32u)
VDAC55 DAC55 0 0
*+ pulse ( 0 3 1u 10n 10n 32u 64u)
VVCV GVCC 0 {vccc}
* 0 pw1 (0 0 10u {vccc})
VVDV GVDD 0 {vccc}
* pw1 (0 0 10u {vccc})
VGGND GGND 0 0
VDVDD DVDD 0 {vccc}
* pw1 (0 0 10u {vccc})

```

g5f_debug.cir

```

VDGND DGND 0 0
VVEE VEE 0 0
VSUB SUB 0 0
VAD0 AD0 0
VAD1 AD1 0
VAD2 AD2 0
VAD3 AD3 0
VAD4 AD4 0
* HTN=3 enables hical
VHTN HTN 0 0
VHOLD HOLD+ 0 3
+ pw1 (0 3 100n 3 101n 0
+ 4.22u 0 4.221u 3
+ 9u 3 9.001u 0
+ 13.22u 0 13.221u 3
+ 18u 3 18.001u 0
+ 23.22u 0 23.221u 3
+ 28u 3 28.001u 0
+ 33.22u 0 33.221u 3
+ 38u 3 38.001u 0
+ 43.22u 0 43.221u 3
+ 48u 3 48.001u 0
+ 53.22u 0 53.221u 3
+ 58u 3 58.001u 0
+ 63.22u 0 63.221u 3
+ 68u 3 68.001u 0
VHOLD- HOLD- 0 1.5
VSTROB+ STROB+ 0 1.4
* + PWL (0 1.4 1U 1.4 1.001U 1.6 10U 1.6 10.001U 1.4)
VSTROB- STROB- 0 1.5
VCMDD+ CMDD+ 0 0
VCMDD- CMDD- 0 1.5
VCMDCV+ CMDCK+ 0 1.4
VCMDCV- CMDCK- 0 1.5
* floaters
VSTI0 N1I293STI0 0 0
VSTI1 N1I293STI1 0 0
VSTI2 N1I293STI2 0 0

```

g5f_debug.cir

```
VN1I293RTNE N1I293RTNE 0 0
VN1I293RTND N1I293RTND 0 0
* VN1I293HTN N1I293HTN 0 3
* M1=3 enables local
VN1I293M1 M1 0 0
* SET VN1I293CS to force HERange
* VCC->HE, GND->LE
VN1I293CS N1I293CS 0 0
VN1I293M4 M4 0 3
VN1I293M5 M5 0 3
RHIZ TDATAOUT 0 1E5
.include gafe5f_xbench.cir
* .include .\n71s.prm
* .include olib_ospice.txt
* .include olib_nanosim.txt
* .include .\t121.mod
.include n84a_prm.txt
* .step param vpk list 0 -.032 -.064 -.096 -.128 -.160 -.192 -.224 -.256
* .step param vpk list -0.064 -0.64 -6.4 -64 -640
* .step param vpk list 0 -1.28 -2.56 -3.84 -5.12 -6.4 -128 -256 -384 -512 -640
* .step param vpk list 0 -.64 -1.28 -1.92 -2.56 -3.2 -3.84 -4.48 -5.12 -5.76 -6.4
* .step param vpk list -5.12 -5.28 -5.44 -5.6 -5.76 -5.92 -6.08 -6.24 -6.4
* .step param vpk list 0 -.064 -.128 -.192 -.256 -.32 -.384 -.448 -.512 -.576 -.64
* .step param vpk list -6.4 -12.16
* .step param vpk list 0 -6.4 -12.8 -19.2 -25.6 -32 -38.4 -44.8 -51.2 -57.6 -64
* .step param vpk list -64 -128 -192 -256 -320 -384 -448 -512 -576 -640
* -7.68 -8.32 -8.96 -9.6 -10.24 -10.88 -11.52
* .step param vmult list 1 0.8 0.6 0.4 0.2 0
* .temp -20 20 50
* .temp 20 -20 -40
* .step param vpk list 0 -5.12 -5.28 -5.44 -5.60 -5.76 -5.92 -6.08 -6.24 -6.4
* .step param vpk list 0 -4.8 -5.12 -5.44 -5.76 -6.08 -6.4 -6.72
* .step param vcc list 3.8 3.6 3.5 3.4 3.3 3.0
* .step param vpk list -0.1 -1 -10
.end
```

GAFE7 Simulation Plot Signal Dictionary

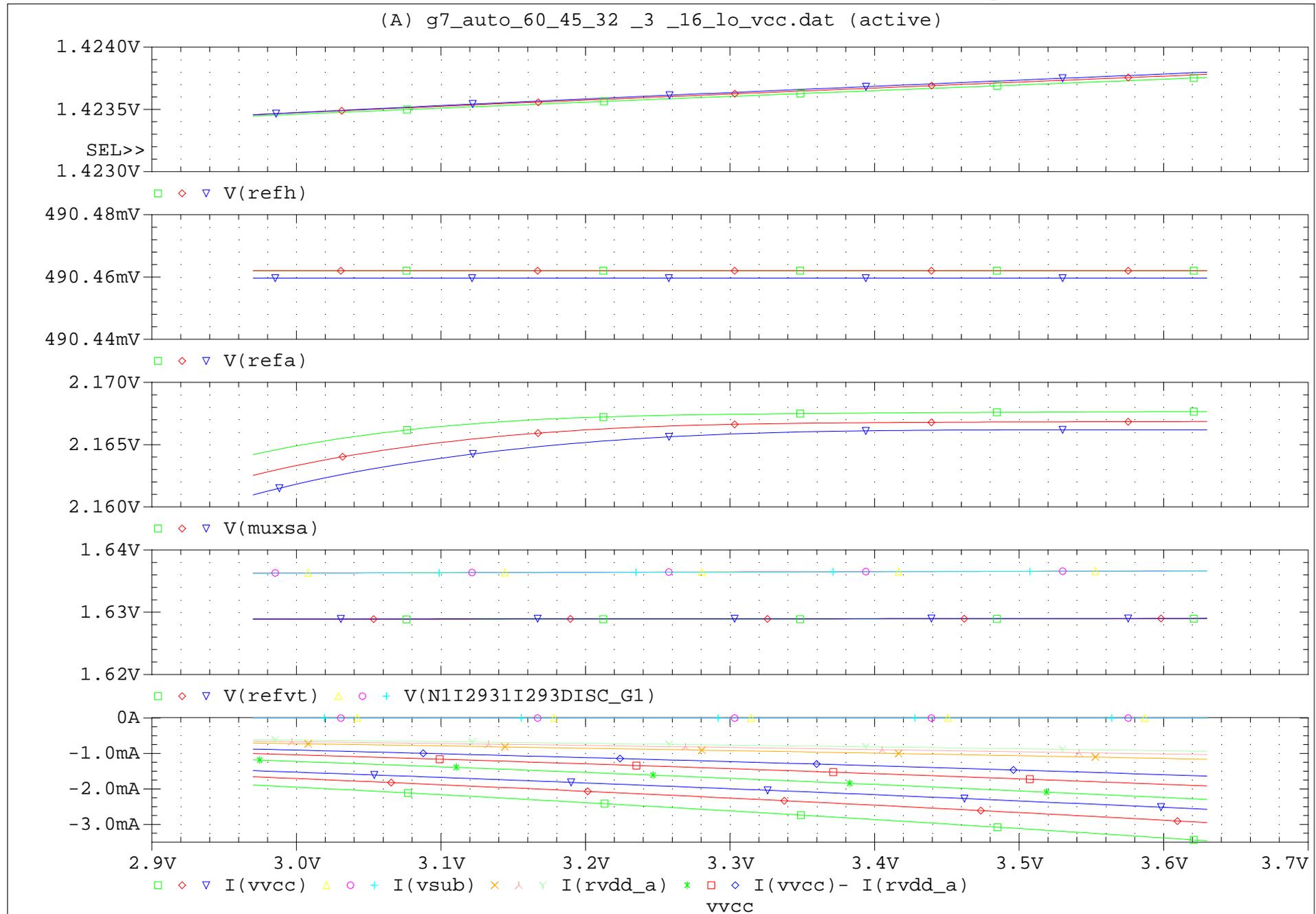
SLAC.OM.20MAY03A

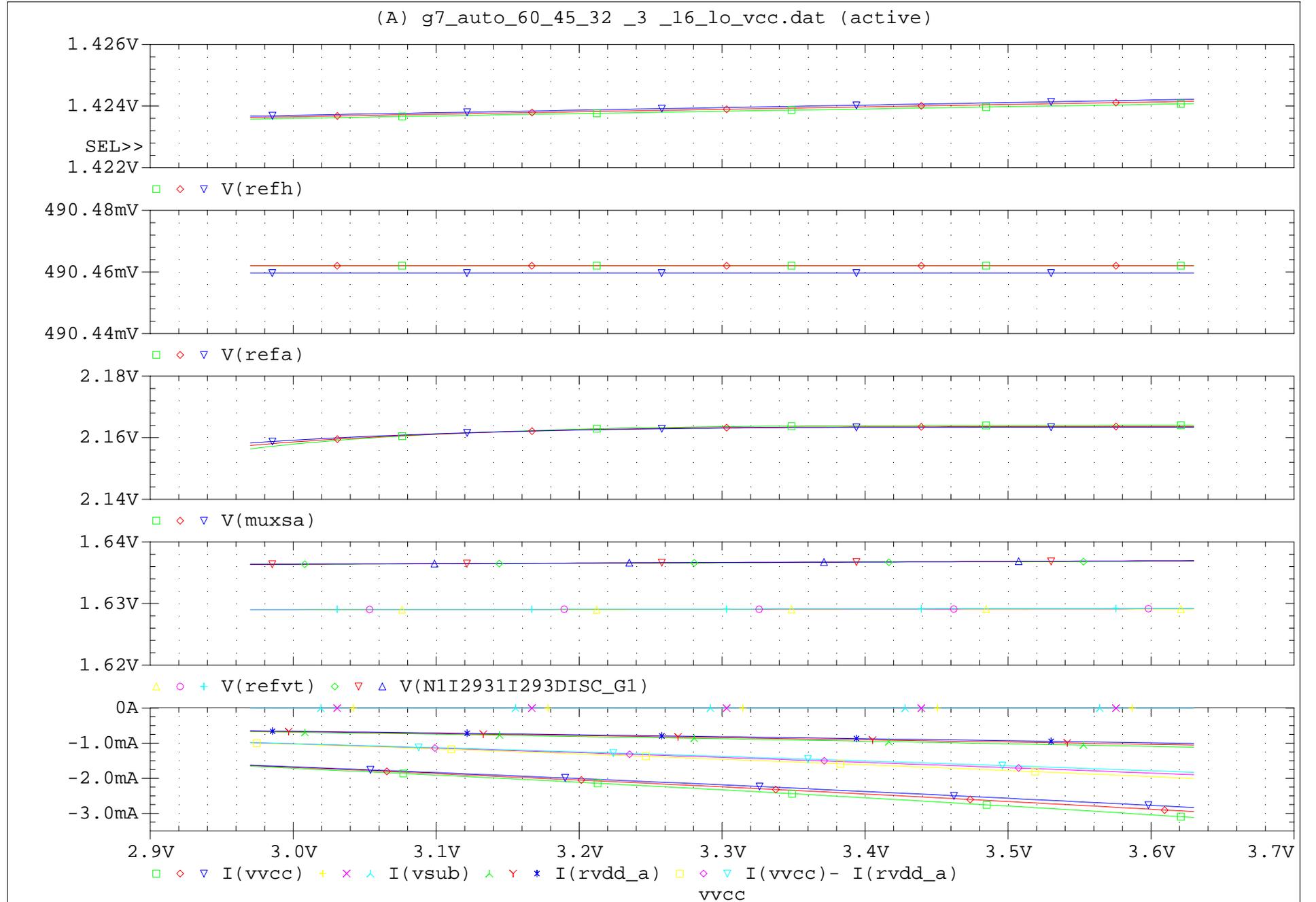
refh	High Energy Threshold
refa	AutoRange Threshold
muxsa	Pulse Height Test Point
refvt	Veto Threshold
n1i2931i293disc_g1	Veto Discriminator Input
vvcc	Analog Power
vsub	Substrate Contact
rvdd_a	Digital Power
tp_vdca	Preamp Baseline
n1i2931i293alo	AutoRange Discriminator Input
discin	High Energy Discriminator Input
muxsh	Pulse Height Out
vt	Veto Out
hd	High Energy Discriminator Output
$\sqrt{s(v(\text{onoise} * v(\text{onoise})))}$	Integrated Spectral Noise Density
onoise	Spectral Noise Density

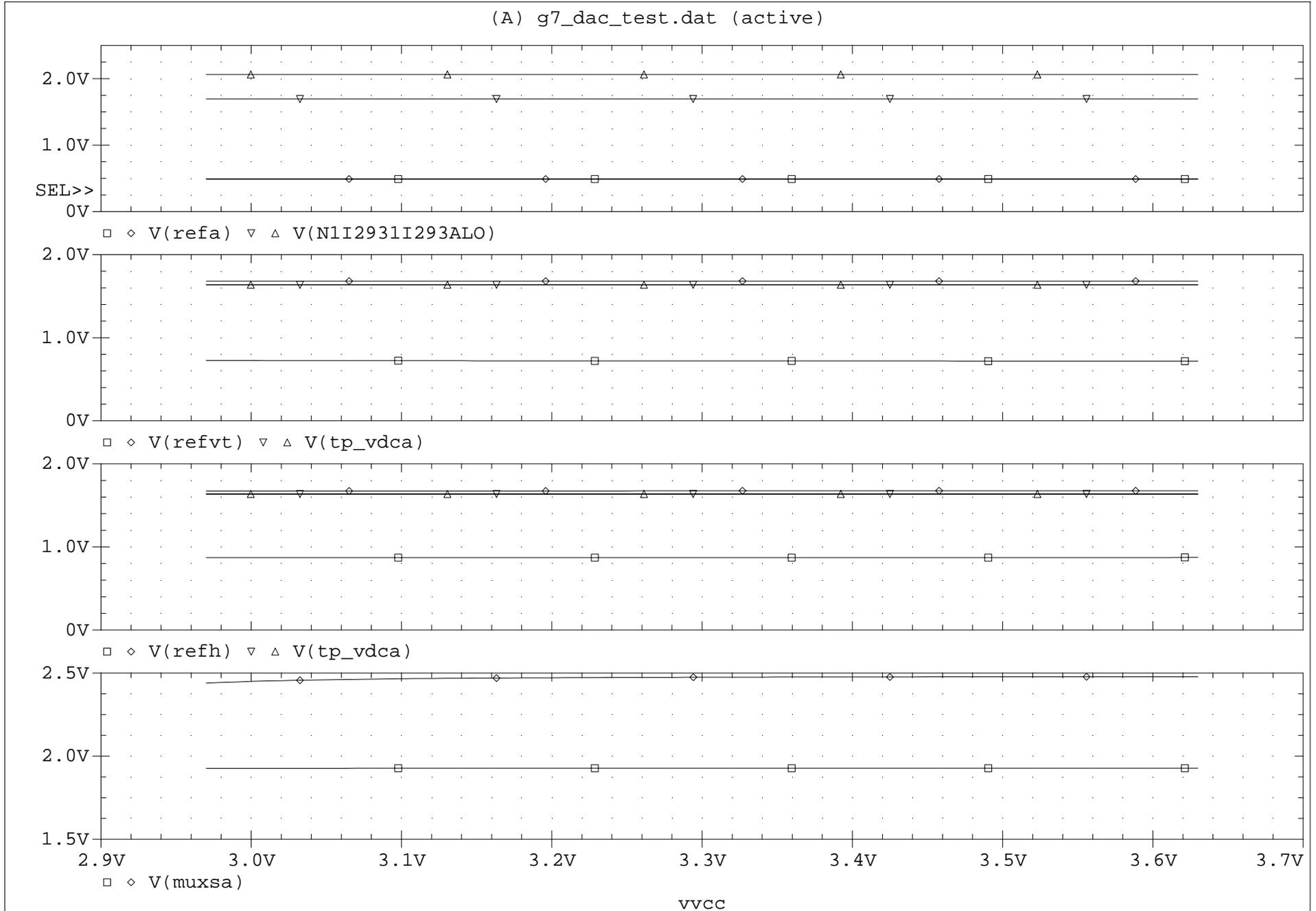
sweep titles and cursors are labeled from left to right

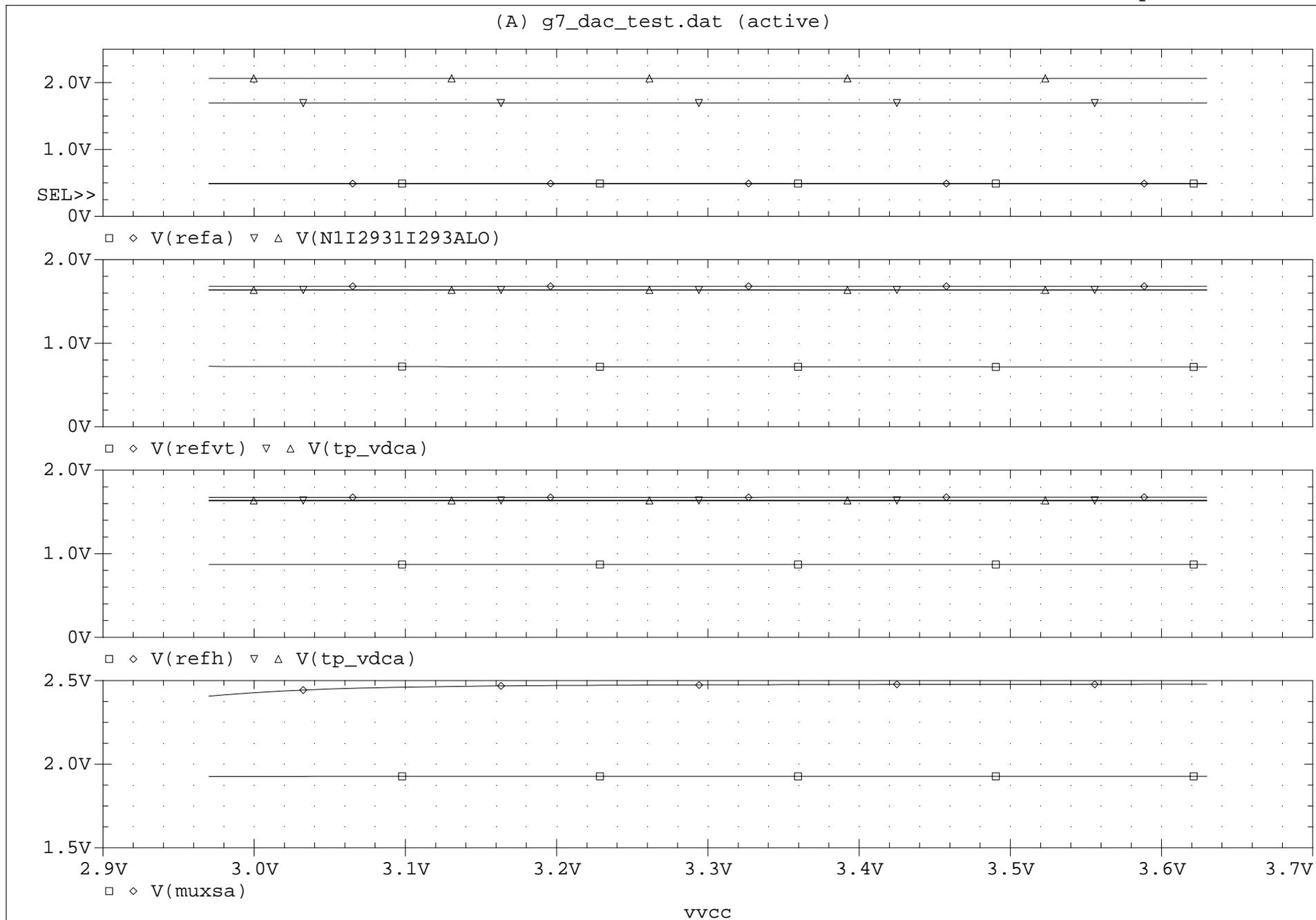
N84A = BSIM Pspice Level 7 Model per MOSIS

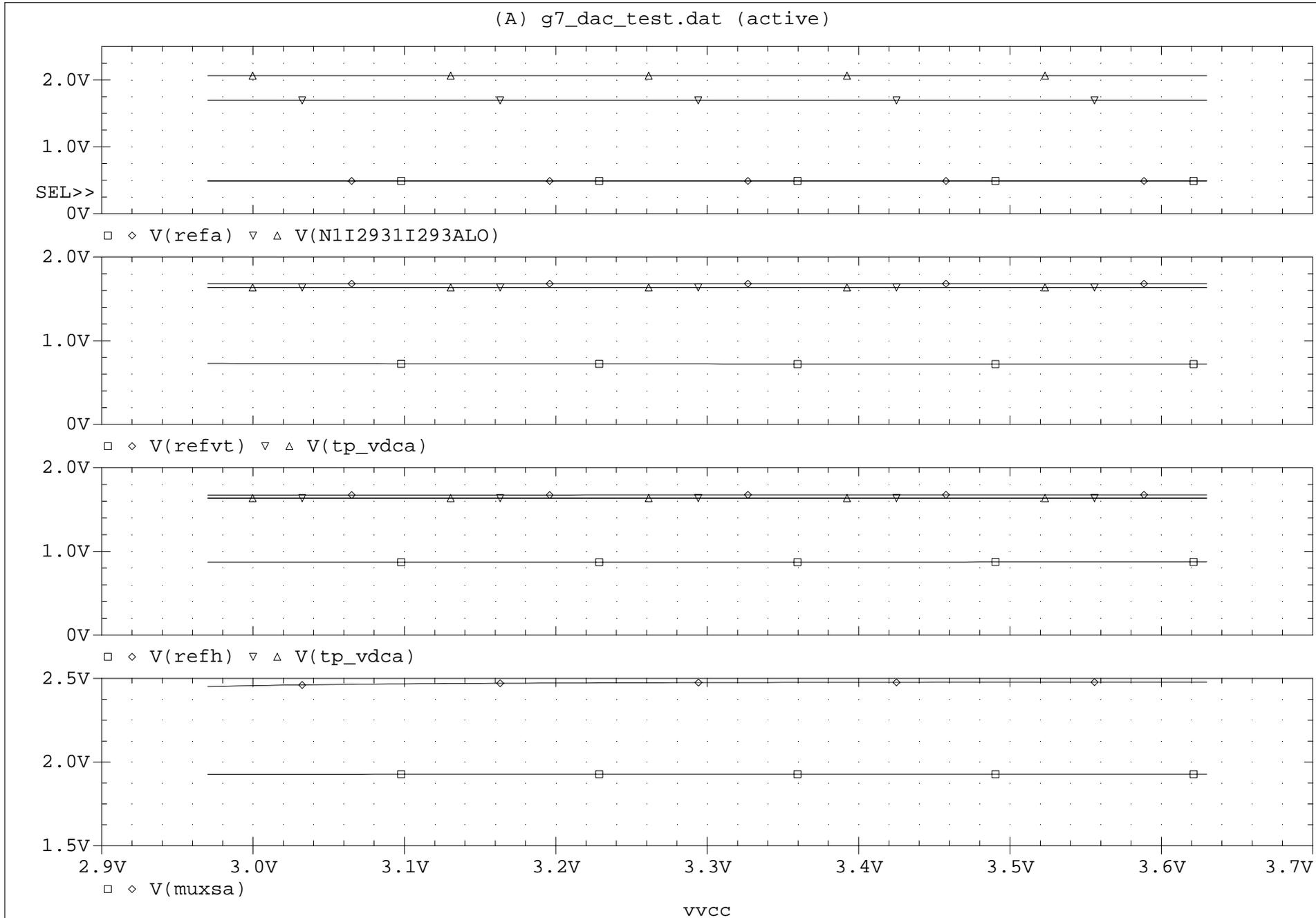
T12L = BSIM Pspice Level 7 Model per MOSIS

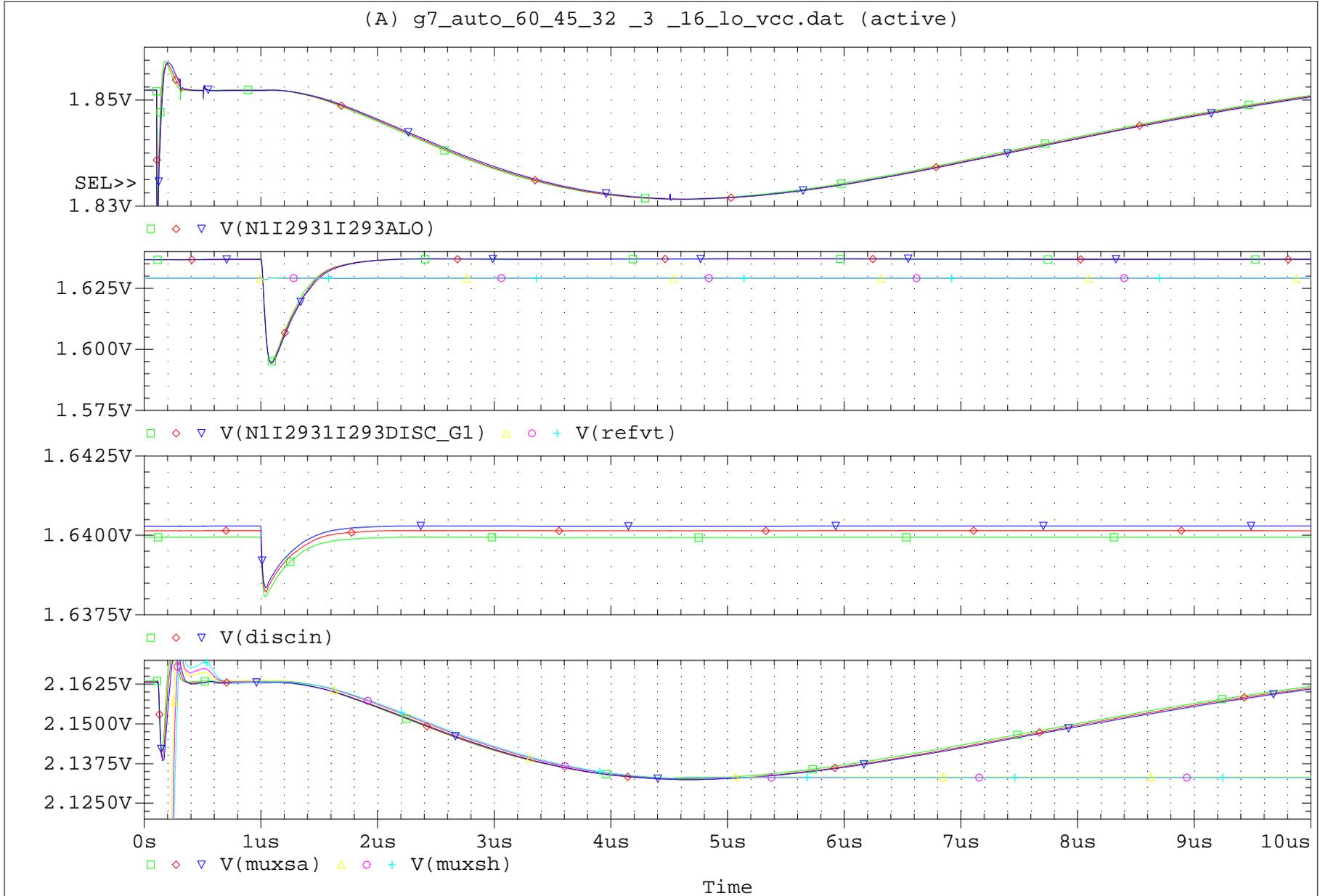


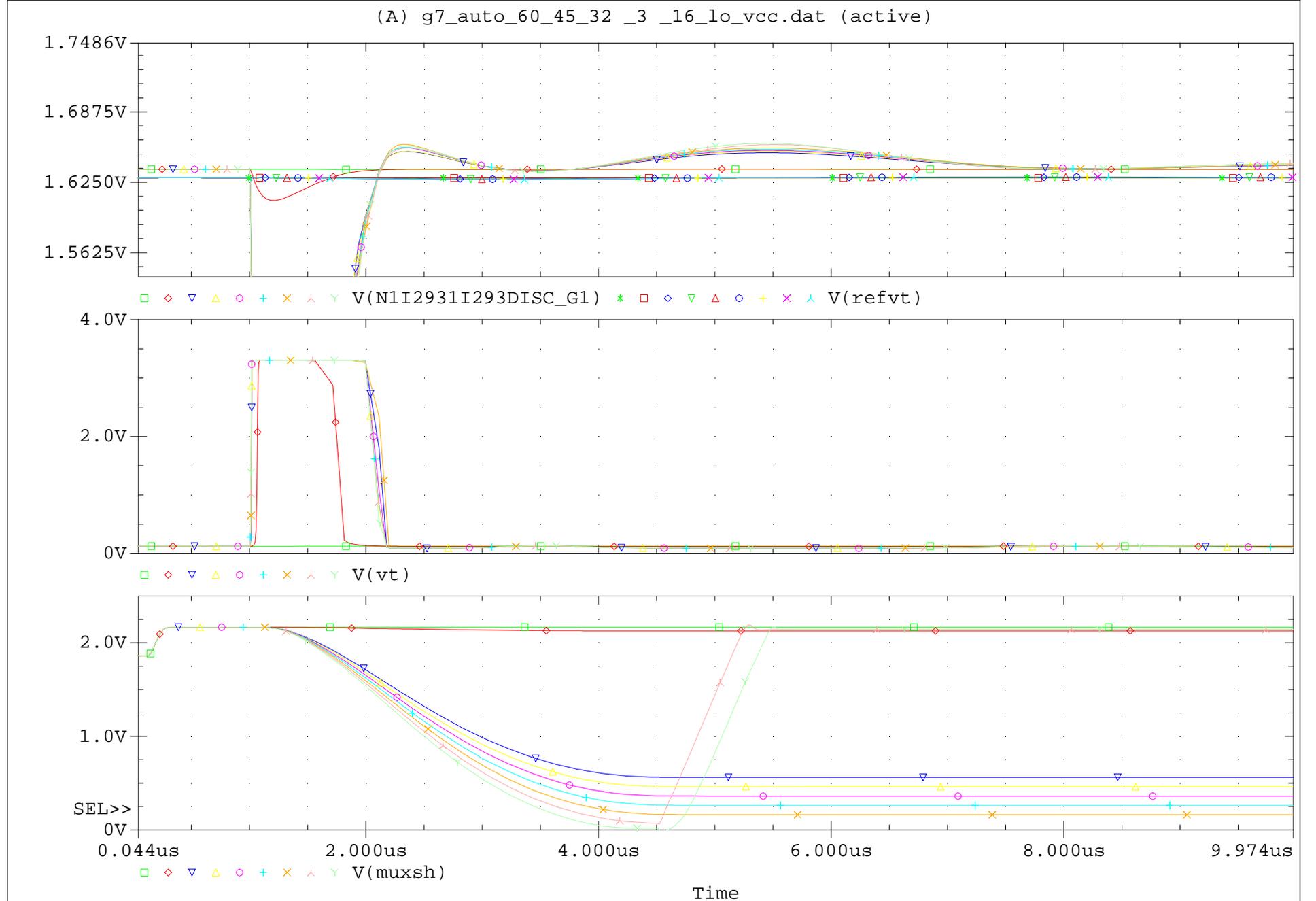


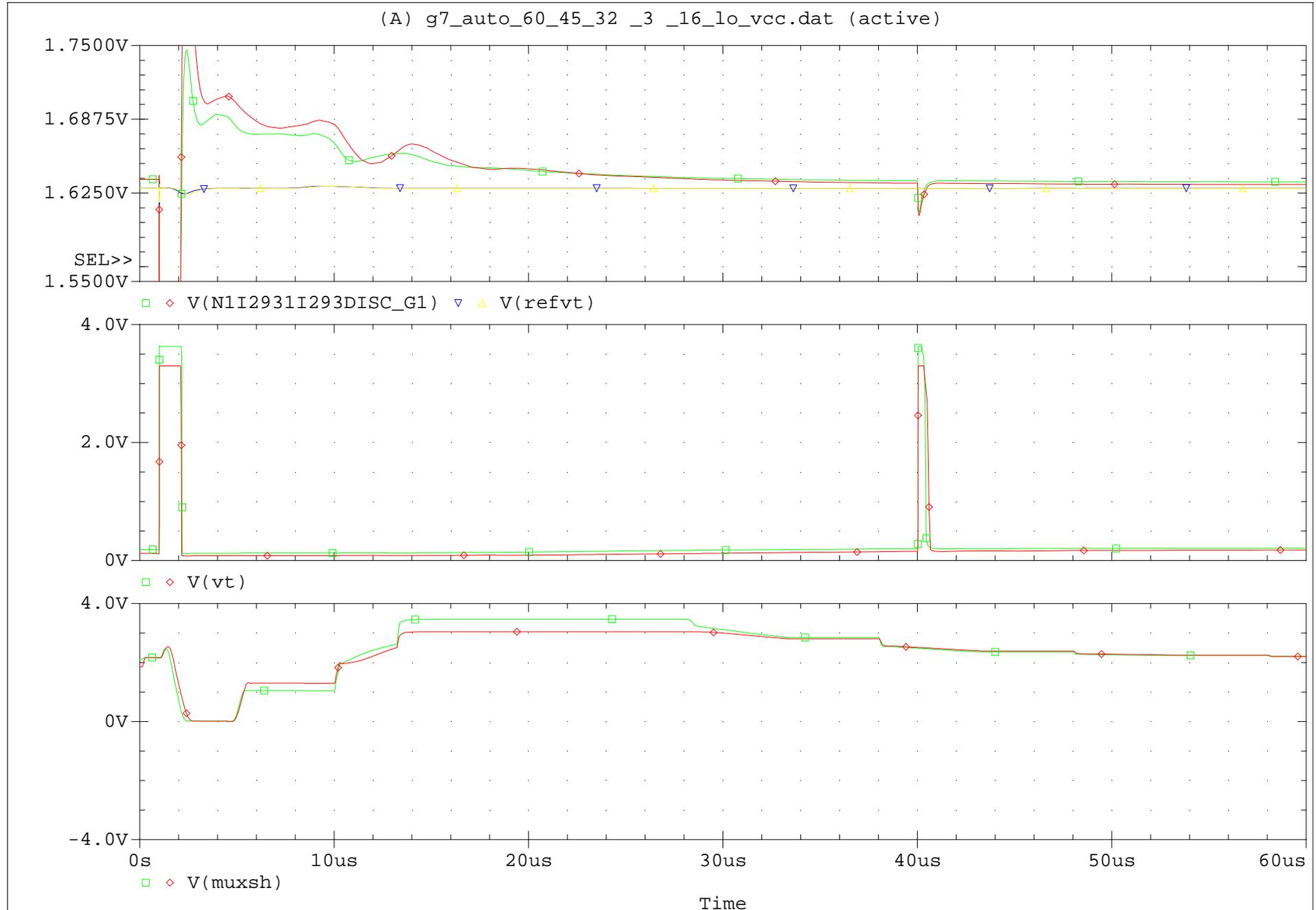


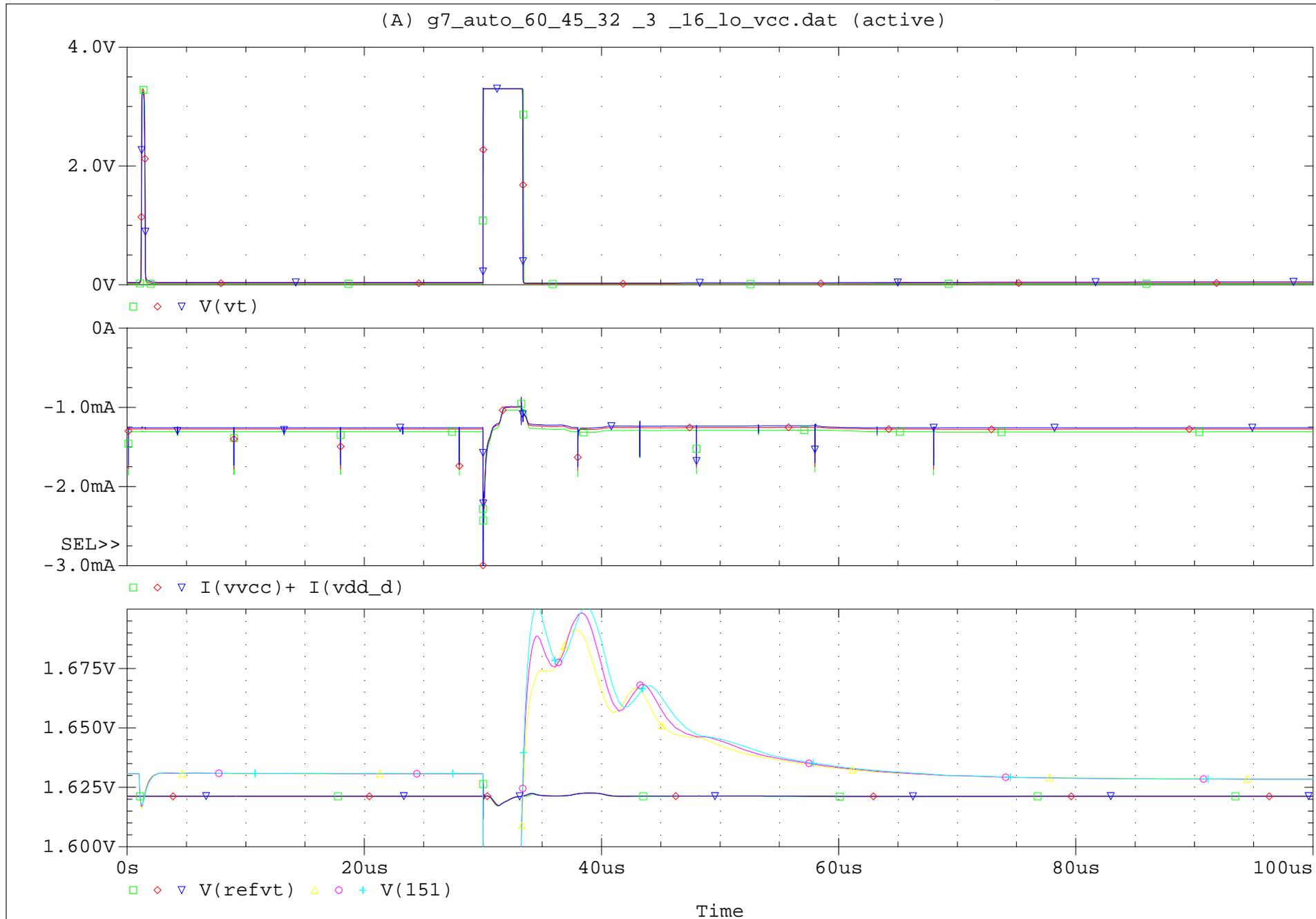


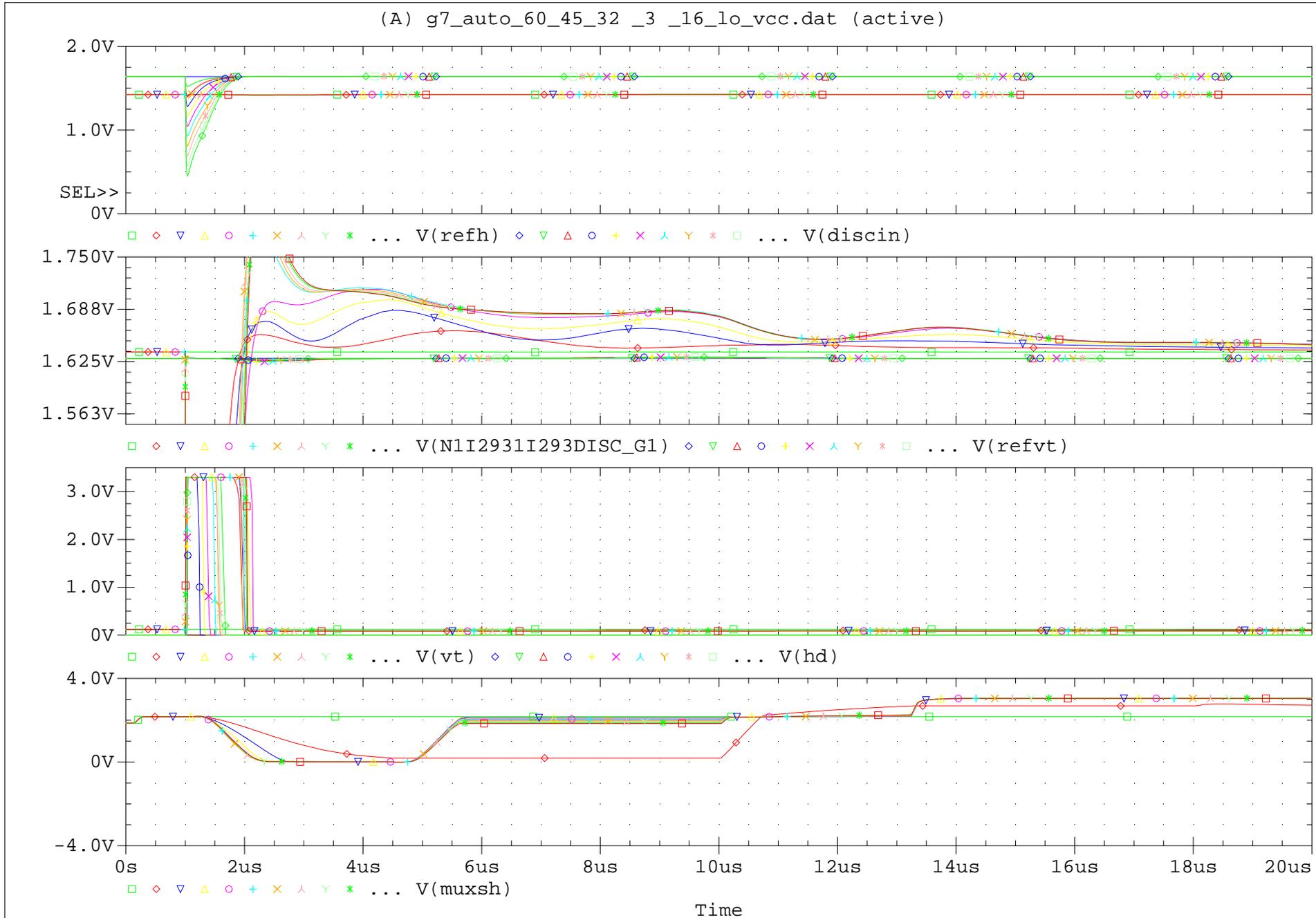


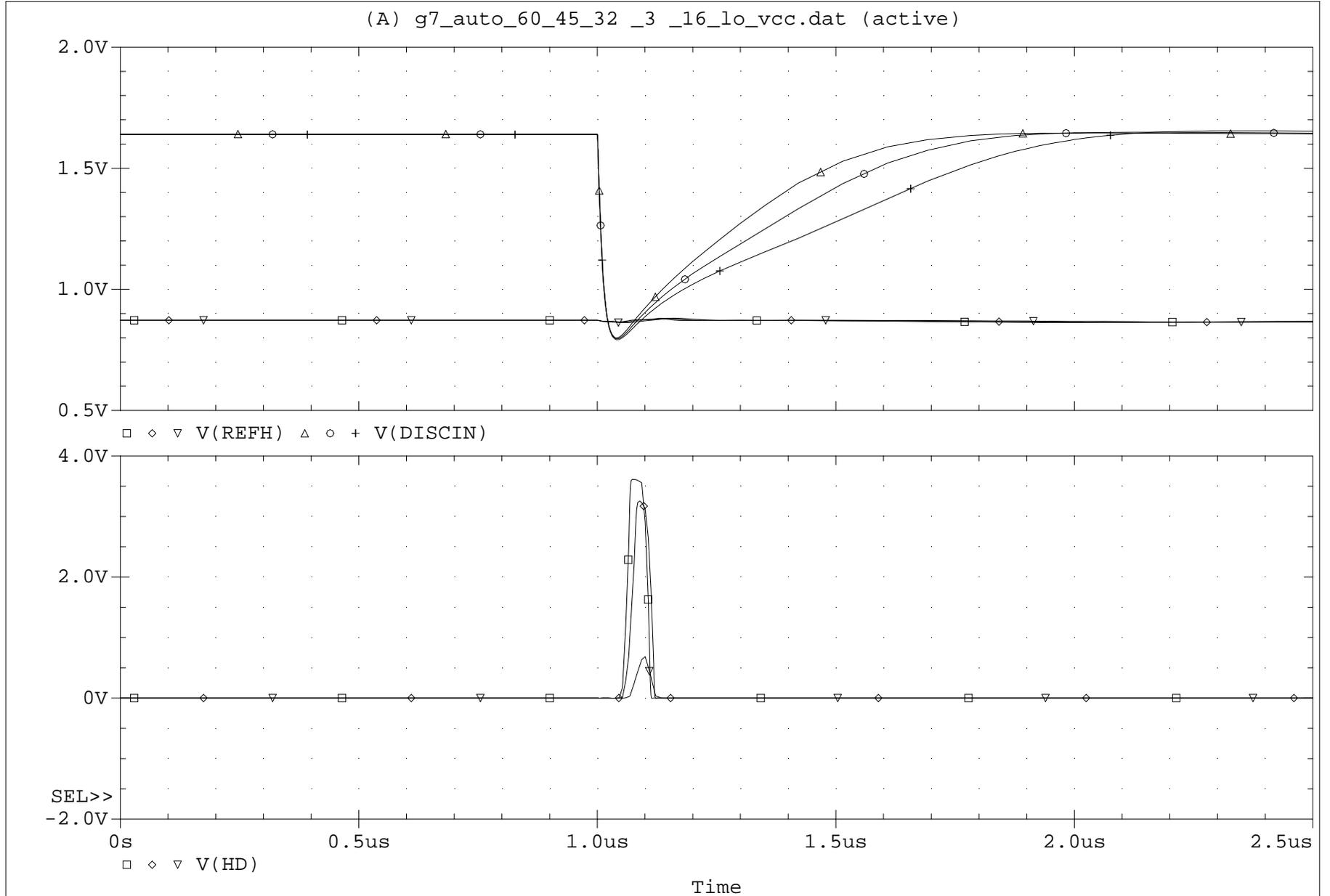


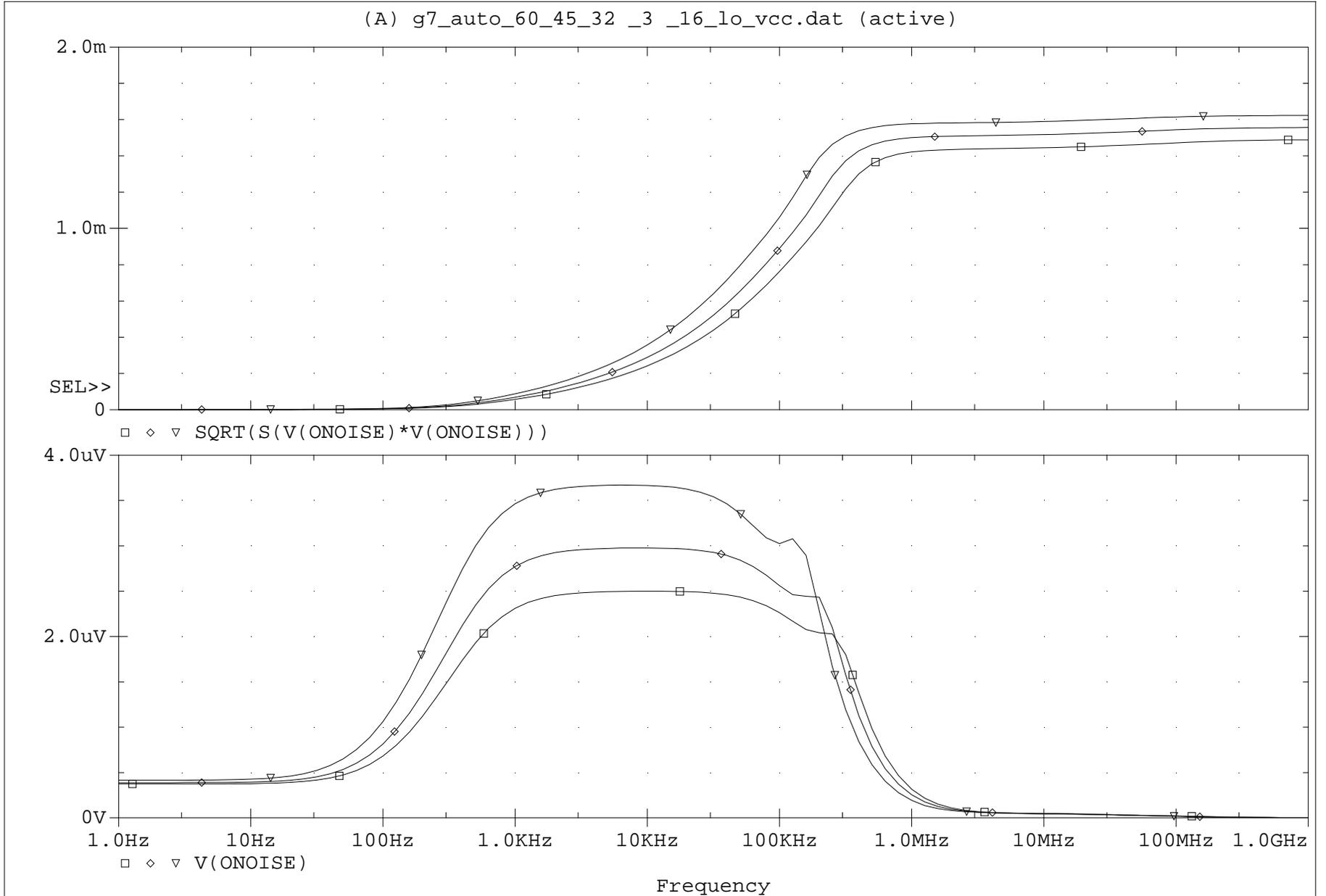


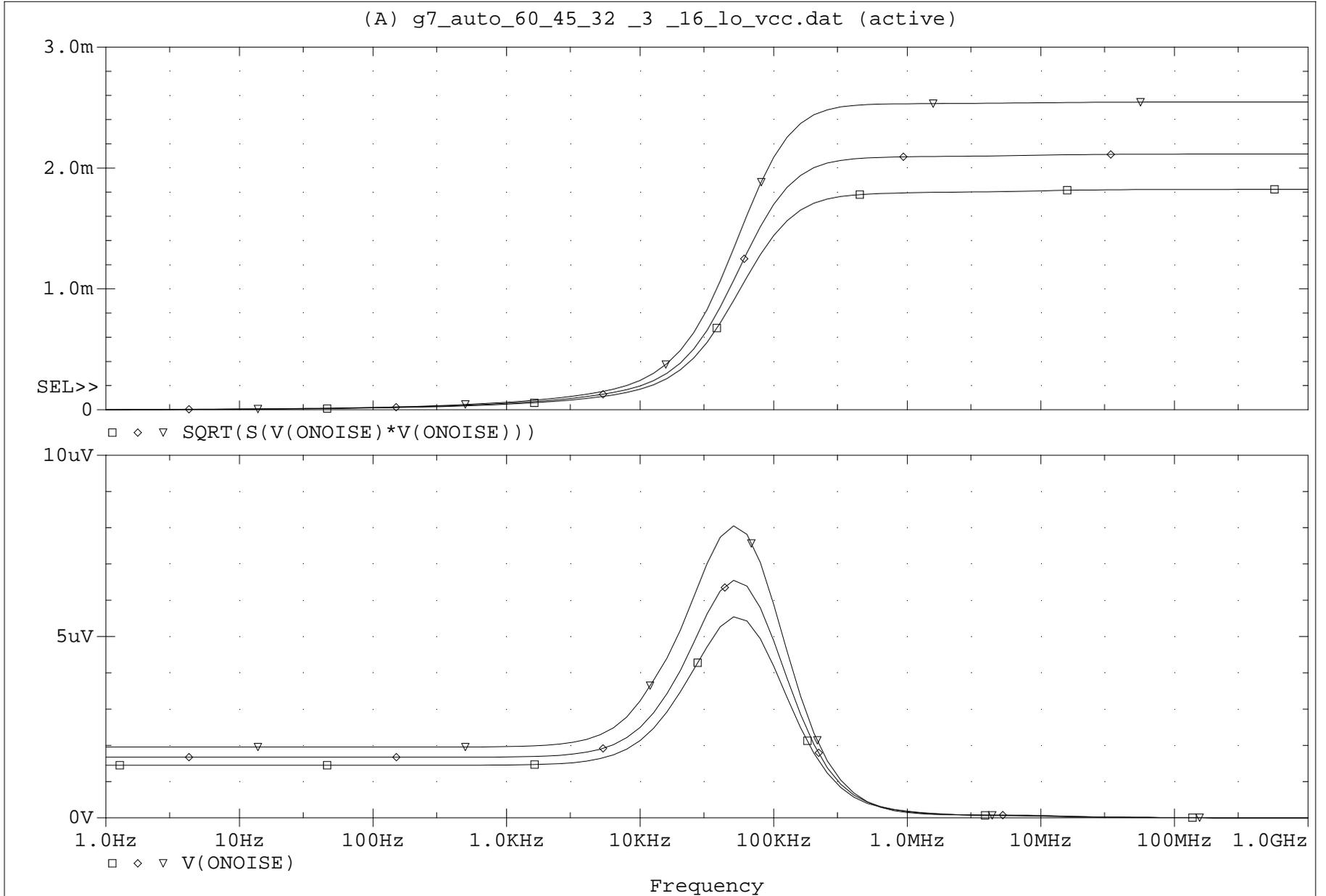


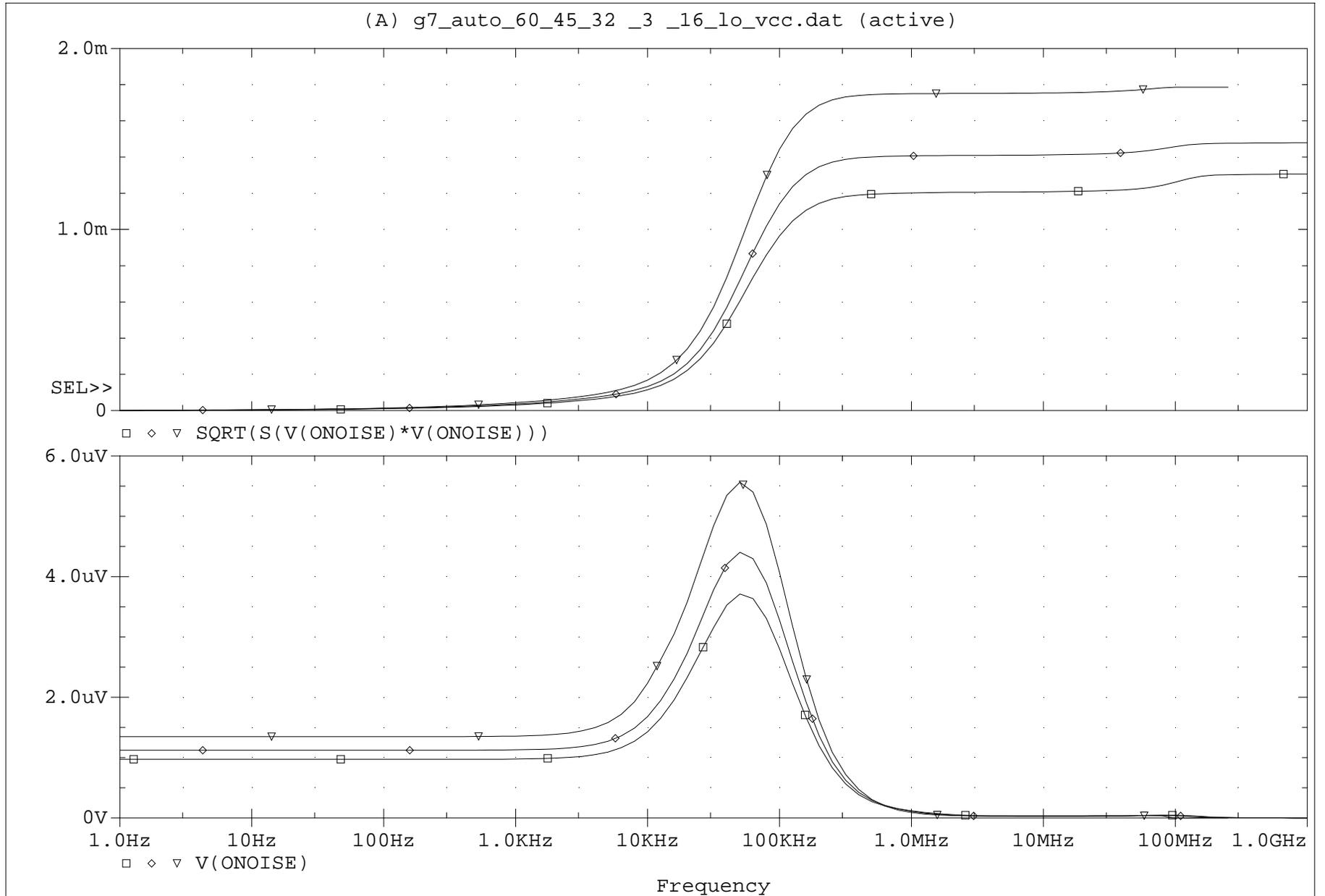


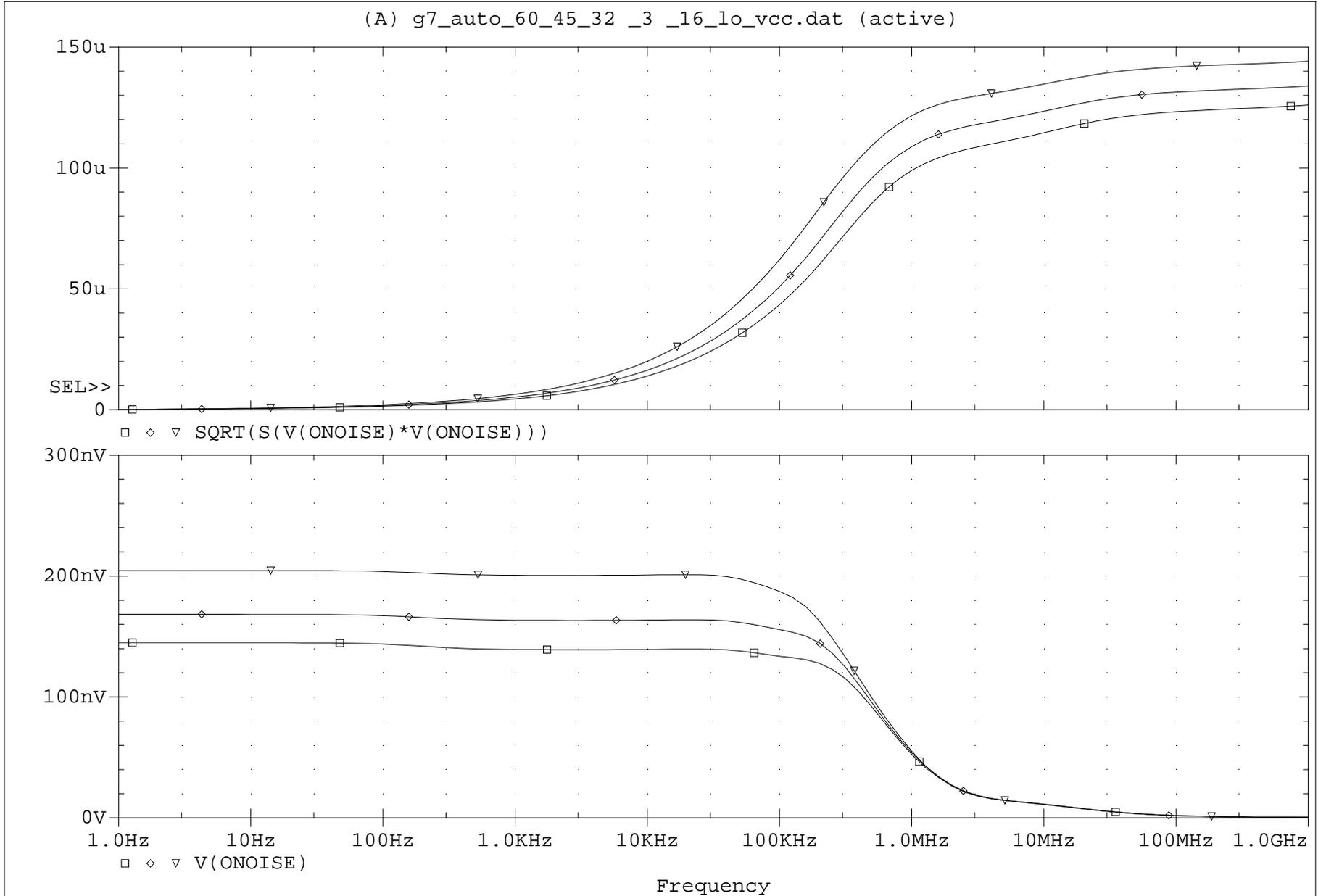


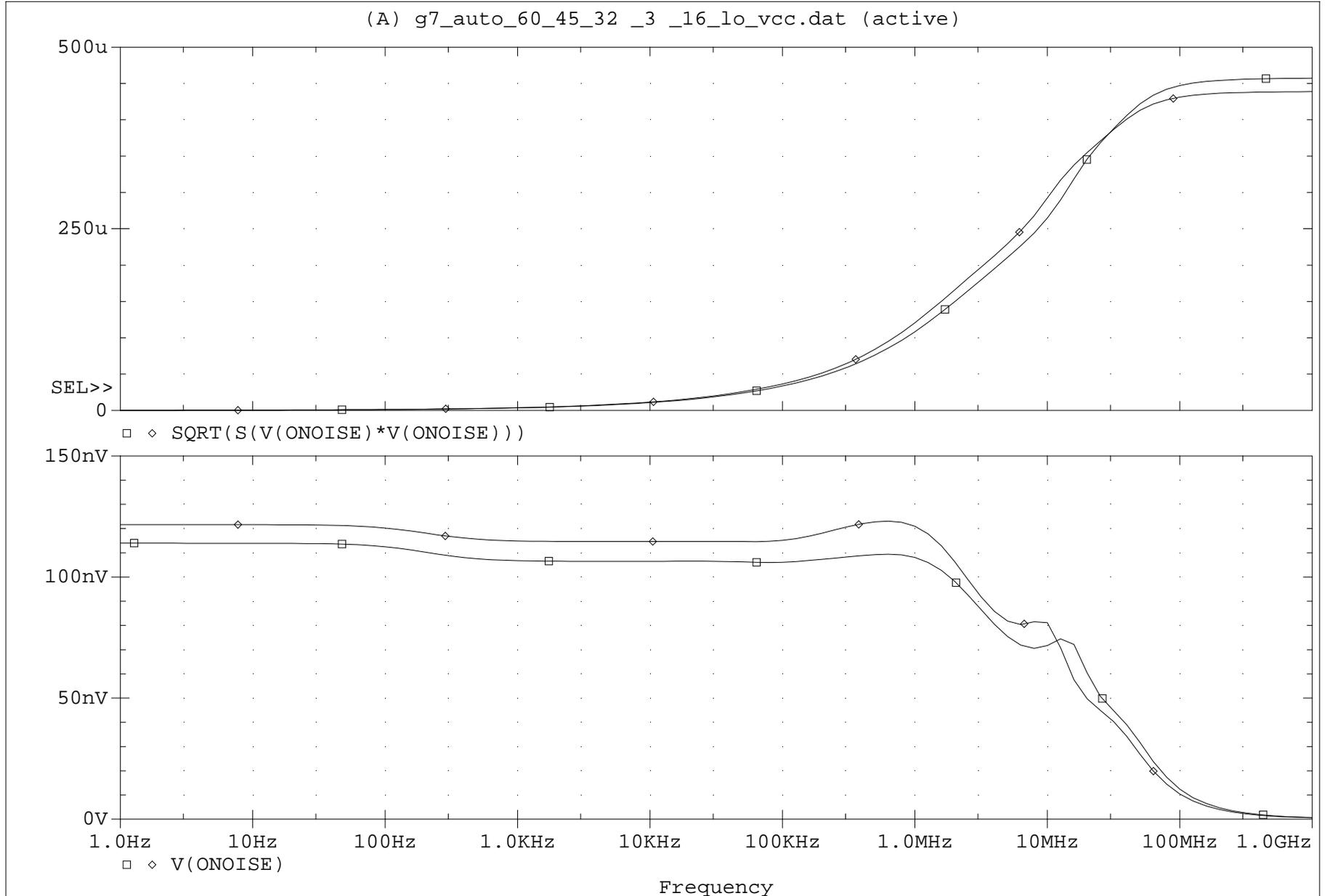












VCC := 2.97 CELCIUS := 20 BSIM_MODEL := N84 GAFE := 7

MIP_SPAN = 9

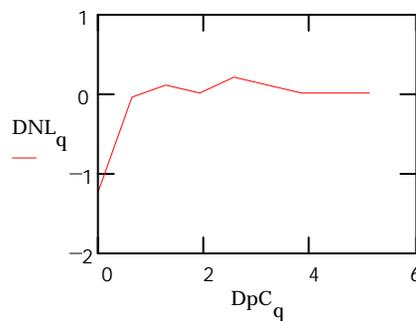
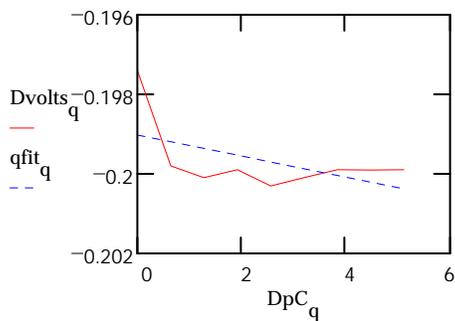
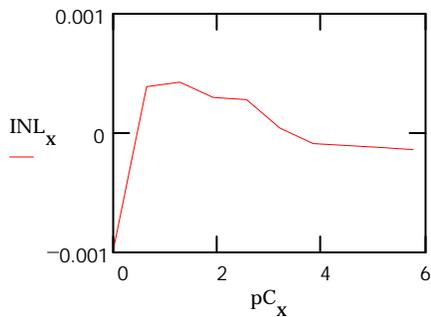
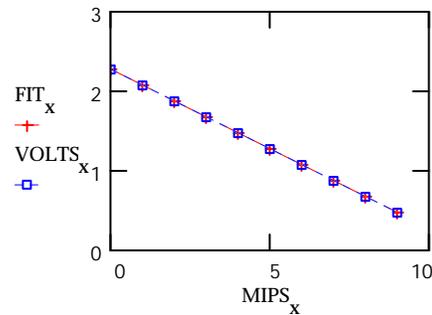
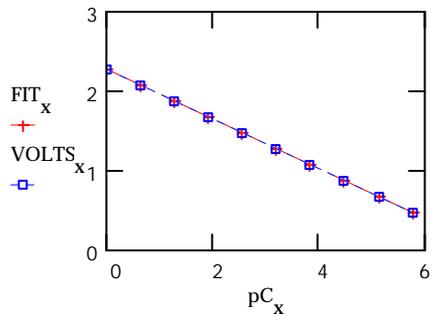
MIP_GAIN = -0.2

OFFSET = 2.28

pC_GAIN = -0.312

INL_SPEC_PCT = 0.141

DNL_SPEC_PCT = 1.451



M =

0	2.278
1	2.081
2	1.881
3	1.681
4	1.481
5	1.281
6	1.081
7	0.881
8	0.681
9	0.481

VCC := 2.97 CELCIUS := 20 BSIM_MODEL := N84 GAFE := 7

MIP_SPAN = 900

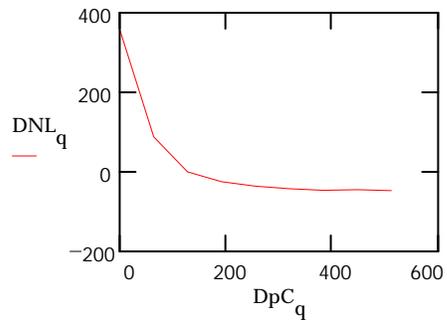
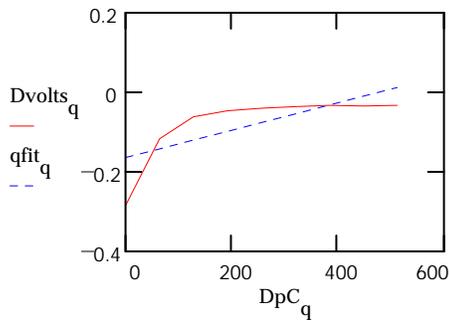
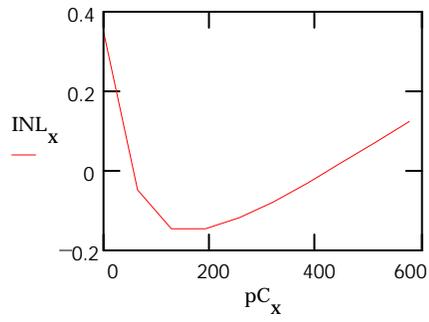
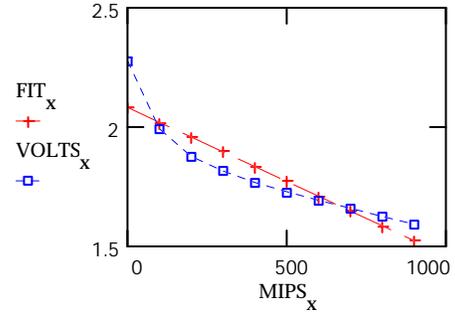
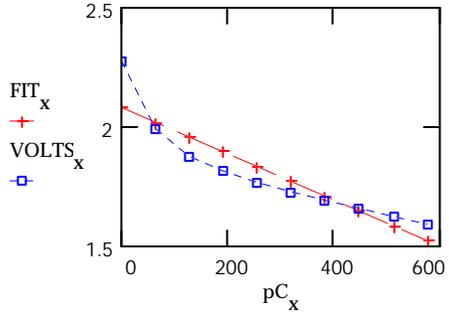
MIP_GAIN = $-6.202 \cdot 10^{-4}$

OFFSET = 2.083

pC_GAIN = $-9.691 \cdot 10^{-4}$

INL_SPEC_PCT = 49.634

DNL_SPEC_PCT = 406.147



M =

0	2.278
100	1.994
200	1.877
300	1.815
400	1.769
500	1.729
600	1.693
700	1.66
800	1.626
900	1.593

VCC := 2.97 CELCIUS := 20 BSIM_MODEL := N84 GAFE := 7

MIP_SPAN = 200

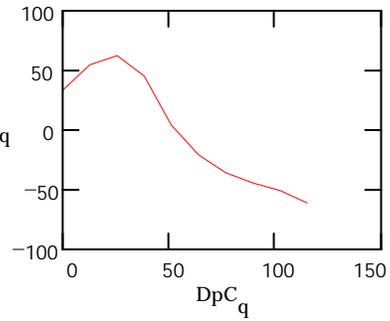
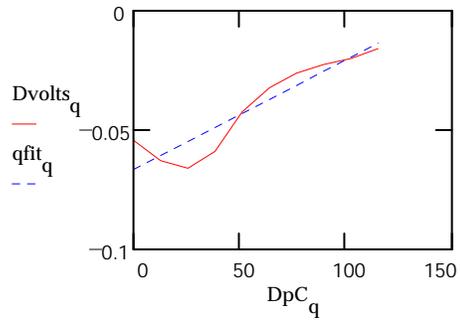
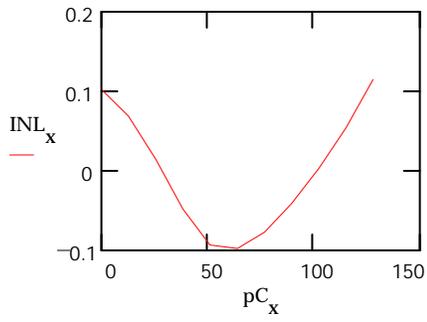
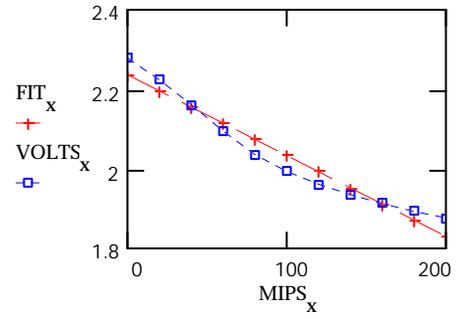
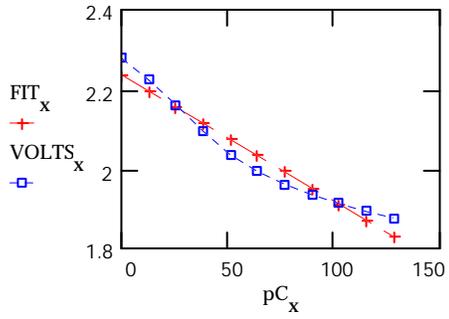
MIP_GAIN = -0.002

OFFSET = 2.237

pC_GAIN = -0.003

INL_SPEC_PCT = 21.274

DNL_SPEC_PCT = 123.568



M =

0	2.278
20	2.224
40	2.161
60	2.095
80	2.036
100	1.994
120	1.962
140	1.936
160	1.913
180	1.893
200	1.877

VCC := 3.63 CELCIUS := 20 BSIM_MODEL := N84 GAFE := 5

MIP_SPAN = 10

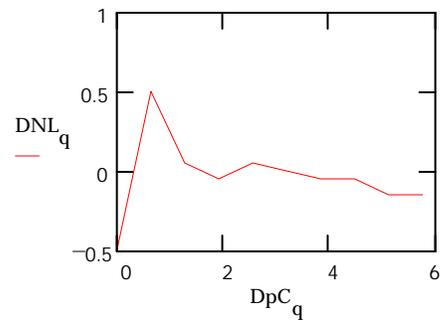
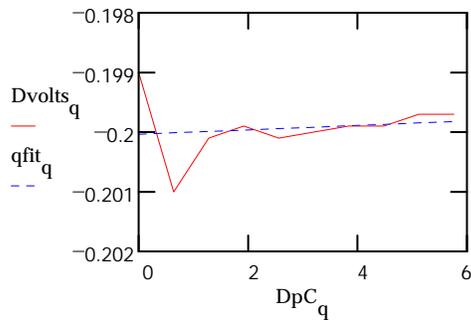
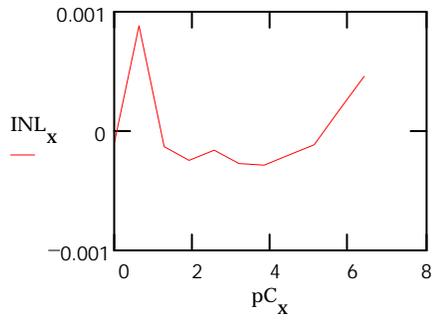
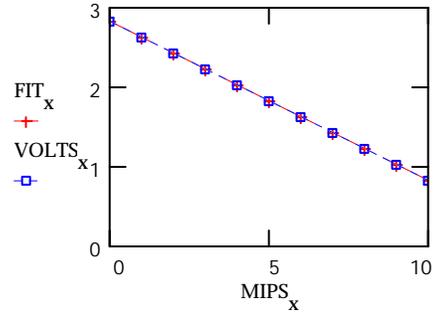
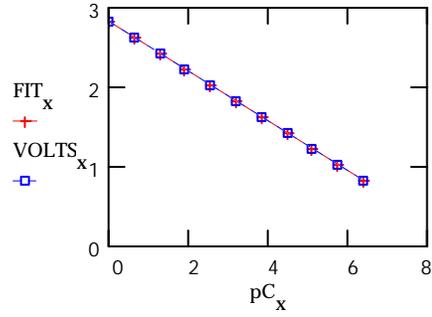
MIP_GAIN = -0.2

OFFSET = 2.832

pC_GAIN = -0.312

INL_SPEC_PCT = 0.058

DNL_SPEC_PCT = 1



M =

0	2.832
1	2.633
2	2.432
3	2.232
4	2.032
5	1.832
6	1.632
7	1.432
8	1.232
9	1.033
10	0.833

GAFE7 Simulated Noise Analysis

SLAC.OM.16May03v1

Node	Integral Noise (mvolts, rms)	Gain (mvolts/MIP)	Input Referred Noise (MIPs, rms)
Veto	1.600	392	0.0041
MuxSA	2.600	200	0.0130
HLD	0.150	14.5	0.0103
AutoRange	1.800	133	0.0135
Veto Threshold	0.400	392	0.0010
HLD Threshold	0.400	14.5	0.0276
Autorange Threshold	0.400	133	0.0030
Quadrature Sums			
Veto	1.649	392	0.0042
HLD	0.427	14.5	0.0295
AutoRange	1.844	133	0.0139

GAFE7 Pulse Height Baseline Offset Analysis

GAFE4 Baseline Spreads...

SN	OS_HE	OS_LE	LE_0	LE_7	HE_0	HE_7
2	362	80	2.456	2.976	2.276	2.791
3	855	254	2.347	2.871	1.976	2.509
7	96	204	2.376	2.877	2.439	2.965
8	577	0	2.517	3.028	2.147	2.662
9	297	144	2.413	2.913	2.315	2.807
12	48	328	2.305	2.816	2.47	2.975

Mean	2.402333	2.9135	2.2705	2.784833 V
Std Dev	0.076644	0.077021	0.185572	0.179067 V, rms
DC Gain	105.6	105.6	105.6	105.6
Input Referred Offset	0.000726	0.000729	0.001757	0.001696 V, rms

GAFE4 DC Gain	220	240	140	105.6
	100	20	35	
	2.2	12	4	

GAFE7 DC Gain	220	255	157	48.39396
	100	35	52	
	2.2	7.285714	3.019231	

Expected DC Spread	0.035124	0.035297	0.085043	0.082062 V, rms
--------------------	----------	----------	----------	-----------------

GAFE7/GAFE4 DC Gain Ratio	0.458276
---------------------------	----------

$$R1 := 100 \cdot 10^3$$

$$R2 := 220 \cdot 10^3$$

$$R3 := 220 \cdot 10^3$$

$$R4 := 35 \cdot 10^3$$

$$R5 := 52 \cdot 10^3$$

$$R6 := 105.3 \cdot 10^3$$

$$C1 := 23 \cdot 10^{-12}$$

$$G1_V_C := \frac{1}{C1} \quad G1_V_C = 4.348 \cdot 10^{10}$$

$$G2 := \frac{R2}{R1} \quad G2 = 2.2 \quad SL1 := 0.5 \quad G2S := G2 \cdot SL1 \quad G2S = 1.1$$

$$G3 := 1 + \left(\frac{R3}{R4} \right) \quad G3 = 7.286 \quad SL2 := 0.6 \quad G3S := G3 \cdot SL2 \quad G3S = 4.371$$

$$G4 := 1 + \left(\frac{R5}{R6} \right) \quad G4 = 1.494 \quad GMIP := .64 \quad GMIP = 0.64$$

$$GT := G1_V_C \cdot G2S \cdot G3S \cdot G4 \quad GT = 3.123 \cdot 10^{11} \quad \text{Volts/Columb at MuxSA}$$

$$R7 := 5.2 \cdot 10^3$$

$$R8 := 135 \cdot 10^3 \quad GV := 1 + \frac{R8}{R7} \quad GV = 26.962 \quad KV := 1 \quad KH := 1$$

$$CQ := 33 \cdot 10^{-12}$$

$$CC := 11 \cdot 10^{-12} \quad GQV := \frac{KH \cdot KV}{CQ + CC} \quad GQV = 2.273 \cdot 10^{10} \quad \text{V/C @ High Level Disc.}$$

$$GTV := GV \cdot GQV \quad GTV = 6.128 \cdot 10^{11} \quad \text{Volts/Coulomb at Veto Discriminator}$$

$$GREF := \frac{GT}{G4} \quad GREF = 2.091 \cdot 10^{11} \quad \text{Volts/Columb at Range Selection Discriminator}$$

$$GMUXSA := GT \cdot 10^{-9} \quad GVETO := GTV \cdot 10^{-9} \quad GAREF := GREF \cdot 10^{-9} \quad GHLD := GQV \cdot 10^{-9}$$

$$MMUXSA := GMUXSA \cdot GMIP \quad MVETO := GVETO \cdot GMIP$$

$$MHL D := GHLD \cdot GMIP \quad MAREF := GAREF \cdot GMIP$$

GAFE7 Gain Predictions:
GMUXSA = mV/pC at MuxSA output
GVETO = mV/pC at Veto Discriminator
GHLD = mV/pC at High Level Discriminator
GAREF = mV/pC at Range Selection Discriminator

GMUXSA = 312.312 GAREF = 209.068
GVETO = 612.762 GHLD = 22.727

In MIP's...

MMUXSA = 199.88 MAREF = 133.804
MVETO = 392.168 MHLD = 14.545

GAFE7 Simulations:
MMUXSA = 200
MVETO=139
MAREF=134
MHLD=11.6

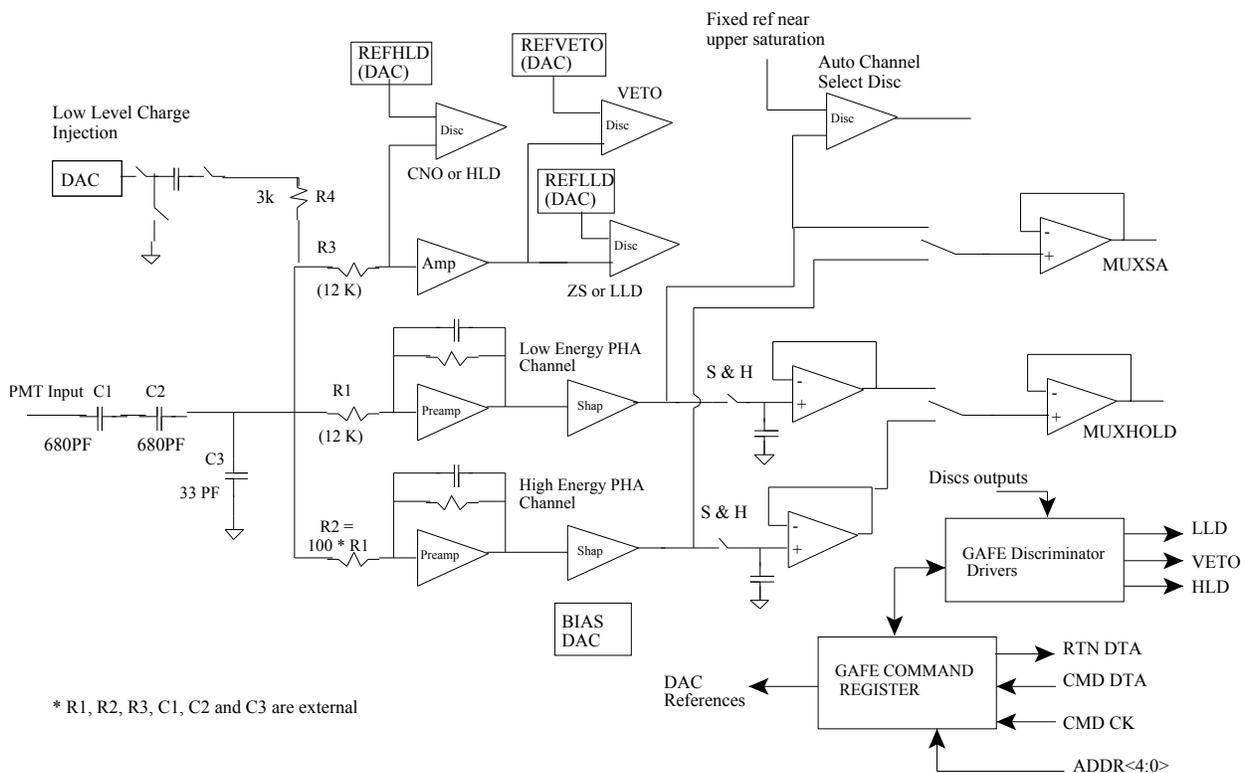
5.2.2.2 Analog ASIC (GAFE)

The primary purpose of the ACD Front End Electronics ASIC is to receive the PMT signal, and process it after suitable amplification to generate fast triggers or discriminator outputs, and shape and hold the signal for Pulse Height Analysis (PHA). The triggers that need to be generated are the VETO, the LLD or ZS, and the HLD or the CNO triggers.

In addition to the above analog circuits, this ASIC also contains the DACs to generate the various thresholds and biases, and also the digital modules which control the mode of operation of the chip and allow it to be interfaced to the outside electronics. The analog and digital subcircuits are described next. A simplified block schematic of the ASIC is given in the figure below.

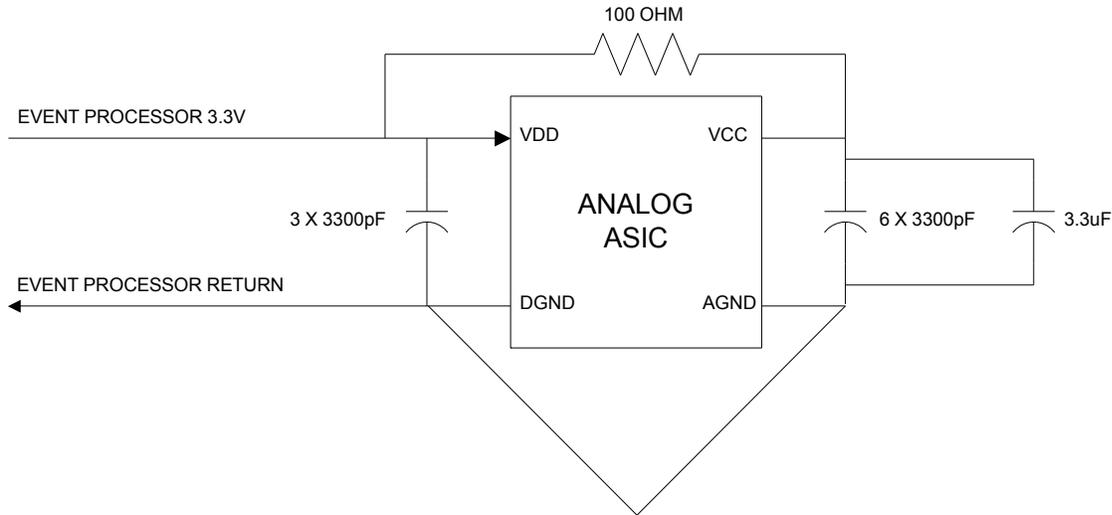
The analog front end comprises mostly of amplifiers and discriminators along with multiplexers, buffers and some other circuit modules. The main requirements that govern the front end electronics design are:

- The dynamic range of 0.1 to 1000 MIP, which for a PMT gain of 400,000, translates to 0.064 PC to 640 PC. The is a dynamic range of 1:10,000.
- Generation of a fast VETO trigger, preferably within 200ns for a 1 MIP signal
- The desired peaking time for the PHA signal is 3us, a shorter time is not desirable as it will lead to greater errors due to timing jitter of the Sample Hold signal.



GLAST ACD Front End (GAFE) Analog ASIC : Conceptual Diagram

The power supplied to the GAFE is as follows:



The +3.3V power from the AEM comes to the FREE circuit card. After local passive filtering on the FREE circuit card, this 3.3V is VDD, the digital power rail. This is locally bypassed with several ceramic capacitors (check with Dave about the values and suitability of 3300 pf caps). The ASICs analog power, VCC, is isolated by a 100-ohm resistor, and locally bypassed by ceramic capacitors and one tantalum capacitor.

5.2.2.2.1 GAFE Level IV Requirements

Detector: PMT, gain = 400,000 The GAFEs anode_output (negative charge) must process signals in the range 0.1 MIP to 1000 MIPS

Charge Range: 0.1 MIP to 1000 MIPS
 instrument dynamic range = 1 : 10,000
 MIP \Leftrightarrow 1 Photo electron (pe) \Leftrightarrow 1.6 E-19 Coulombs
 dynamic range = 1.6E-19 C to 1.6E-15 C

Detection of Charged Particles (L3 – 5.2): Generate a trigger output for signals above a nominal threshold of 0.3 MIPS

VETO Threshold (L4 – 5.3): Adjustable from 0.1 MIP to 2.0 MIP with a step size of 0.05 MIP or a charge range of 0.064pc to 1.28pc with a step size of 0.032PC

Veto Trigger Latency: latency for the entire ACD electronics chain shall be greater than 100 ns and less than 600ns from the time of particle passage., The minimum latency expected is 150ns and is not likely to be less than 50ns. The jitter on the Veto trigger shall be less than or equal to 200 ns.

VETO Duration: longer than the time for baseline recovery to 0.05 MIP (for a 2.0 volt signal amplitude that is generated from a 10 MIP signal.)

Recovery to 1 MIP: For 1 MIP signal, VETO should be no longer than 1.2us

Recovery to Large Signals (1000 MIPS): VETO should be no longer than 10 us

VETO Signal Retrigger (Pulse Pile Up !) : To be retriggerable within 50ns of the trailing edge.
(This should be handled by a VETO stretching Logic as described in the following text, this logic will be outside the ASIC)

CNO or HLD or High Level Threshold Detection: nominal threshold of 25 MIPS

CNO or HLD Threshold: Adjustable from 20 to 64 MIPs in steps of less than or equal to 1MIP

CNO or HLD Latency: latency no more than that of VETO signal.

LLD or ZS (Low Level Threshold or Zero Suppress) Signal: nominal threshold of 0.1 MIP

LLD or ZS Threshold: Adjustable from 0.05 MIP to 1 MIP in steps of 0.05 MIP

PHA (Pulse Height Analysis) output:

Low Energy / High Gain Channel:

Range: 0 to 10 MIPs

Resolution: 0.1 MIP to 10 MIPs with a precision of 0.02 MIP or 5% which ever is larger

High Energy / Low Gain Channel:

Range: 0 to 1000 MIPs

Resolution: for pulses above 20 MIPs and up to 1000 MIPs, a precision of 1 MIP or 2% which ever is larger

Test Charge Injection: ASIC to have mechanism for injecting test charge at the front end of electronics chain, the maximum injected charge will be 40pc (16pf * 2.5v), which corresponds to 62.5 MIPs.

Digitization: 10 or 12 bit ADC outside ASIC

5% Integral Non Linearity acceptable

PMT Rise Time: for signal out of PMT : 3-5ns, 1ns for faster tubes

Event Rate: < 3 KHz per PMT

<= 5% of PMTs are expected to be digitized on an average

The various blocks of the analog circuit which are shown in Fig. ??? are discussed next

5.2.2.2 Amplifier with Charge Splitting

The ACD requirements of 0.1MIP to 1000 MIPs dynamic range is too large to be handled by one channel of electronics with a fixed gain. To ease this requirement on electronics, the electronics are split into two channels, a high gain channel that can measure up to 10 MIPs, and a low gain channel that can measure up to 1000 MIPs. In this approach two preamplifiers are used and each has a series resistance at the input to the PMT. The charge that goes into each of the preamplifiers is inversely proportional to the resistance. This technique is used to handle a wide dynamic range such as required here.

In addition to the charge splitting resistances, an external cap of 33 pF is used. The two charge splitting resistances bleed the capacitor's charge. The resistors are in series with two amplifiers. The amplifiers are part of a slow shaping circuit that is required for PHA. The voltage signal developed across the capacitor is fed to the input of the discriminator through a series resistance. For this approach, the charge splitting resistors and capacitors are external to the GAFE.

5.2.2.3 Input Charge

The design requirement calls for handling a signal range from 0.1 MIP to 1000 MIPs. A signal of 0.1 MIP generates 1 photoelectron (pe), which has a charge of 1.6E-19 Coulombs (C). Therefore, for a full scale input of 1000 MIPs, the charge generated is 1.6E-15 C. Since the gain of the PMT is 400,000, the charge input to the ASIC is, 0.064PC for 0.1 MIP, and 640 PC for 1000 MIPs. For a charge collection capacitor of 33 pF, the signal developed across it as required by the various discriminators is as follows:

0.1 MIP <=> 0.064 PC <=> 1.94 mV
1 MIP <=> 0.64 PC <=> 19.4 mV
10 MIPs <=> 6.4 PC <=> 194 mV

30 MIPs \Leftrightarrow 19.2 PC \Leftrightarrow 582 mV
50 MIPs \Leftrightarrow 32 PC \Leftrightarrow 970 mV

The choice of 33 pF for the external charge collection capacitor therefore seems to be adequate as the voltage generated across it is within the input range of all the discriminators.

5.2.2.2.4 High Voltage Coupling Capacitors

Since the charge is collected across a capacitor of 33 pF, the high voltage capacitors should be much larger than 33 pF. Using two 680 pF capacitors in series for high voltage decoupling is adequate.

5.2.2.2.5 Input Time Constant and Discriminator Output Duration

The design requirement for the fast VETO signal is 1.2 μ s for a 1 MIP signal. Therefore, the longest VETO duration obtained for the minimum threshold of 0.1 MIP is given by the equation,

$$0.1 \text{ MIP} = 1 \text{ MIP} * \exp^{-1.2\mu\text{s}/\tau} \Rightarrow \tau = 0.43 \mu\text{s}$$

Therefore, the time constant chosen for a signal going into the discriminators is 400 ns. This implies that the series resistance to the input of the low energy Shaping amp is given by,

$$r1 = 400 \text{ ns} / 33 \text{ pF} = 12 \text{ k}\Omega$$

5.2.2.2.6 Charge Splitting Resistors

As discussed above, the input resistor to the High gain or the Low Energy channel is 12 k Ω . The High Energy channel has the full scale of 1000 MIPs, which is 100 times the full scale of Low energy channel. The series resistance to the High energy channel's input is chosen as 100 times that of the resistance in the Low energy channel and is 1.2 M Ω .

5.2.2.2.7 Shaping Time for Pulse Height Amplifiers

The latency of the sample and hold from the LAT is 2 μ s. Therefore, the minimum peaking time of the shaped pulse is 2 μ s. However, the resistor and capacitors that are fabricated in silicon can vary by 20% from one run to another and in the x and y direction. As a result, the peaking time has been increased by $2 \mu\text{s}/0.8/0.8 = 3.125 \mu\text{s}$.

5.2.2.2.8 Fast Channel Amplification

Where the VETO and Low Level (LLD) discriminators trigger, the signal range is small. The signal across the input capacitor is first amplified by a gain of 20 before being input to the VETO and LLD comparator circuits. With reference to 3.3 volts, a 0.1 MIP signal after amplification of 20 would now correspond to approximately 40 mV. That is large enough to trigger the comparator.

The input to the High Level (HLD) or CNO discriminator is not amplified, as the signal is already large enough.

5.2.2.2.9 Low Level Test Charge Injection

An on chip capacitor of approximately 16 pF has been fabricated. For a 2.5 v input, this would allow charge injection of 40 PC or 62.5MIPs. When not in use, the charge injection capacitor is disconnected by a switch that is activated by the Test Enable signal.

5.2.2.2.10 Zero Suppression and Low Level Discriminator

The threshold of this discriminator is set by a signal labeled, "REFLLD". Since the signal is negative going at the discriminator input and is at a base line of vdc1 (approx 1.5v), the reference is set to a level below

vdc1. Therefore for zero level threshold setting, the reference should be set to vdc1 and for increasing signals; it should be decreased towards zero volts. The threshold setting is done by on chip DAC.

5.2.2.2.11 VETO Discriminator

The threshold of this discriminator is set by signal labeled, “REFLLD”. Since the signal is negative going at the discriminator input and is at a base line of vdc1 (approx 1.5v), the reference is set to a level below vdc1. Therefore for zero level threshold setting, the reference should be set to vdc1 and for increasing signals; it should be decreased towards zero volts. The threshold setting is done by on chip DAC.

5.2.2.2.12 High Level Discriminator or CNO

The threshold of this discriminator is set by signal labeled, “REFHLD”. Since the signal at the discriminator input is at a base line of vdc1 (approx 1.5v), the reference is set to a level below vdc1. Therefore for zero level threshold setting, the reference should be set to vdc1 and for increasing signals, it should be decreased towards zero volts. The threshold setting is done by on chip DAC.

5.2.2.2.13 PMT Gain Drift

There is no gain adjustment on the ASIC. However, the gain of a group of PMTs is increased by increasing the high voltage so that the gain of the weakest PMT in that group is brought back up to the nominal level. To take care of the PMT gain variation from channel to channel, the threshold of the various discriminators for each channel or PMT are individually set by the on chip DACs.

A one time gain adjustment of the electronics chain is also possible by suitably selecting the external charge collection capacitor which is to be implemented on the board as a parallel combination of two capacitors.

5.2.2.2.14 Low Energy Pulse Height Analysis Channel

The low energy signal is amplified, shaped to peak at 3 μ s and feeds a sample hold circuit which is operated when a Hold signal is delivered from external to the chip.

5.2.2.2.15 High Energy Pulse Height Analysis Channel

The high-energy channel is similar to the low energy channel. The signal is amplified, shaped to peak at 3 μ s and feeds a sample hold circuit which is operated when a Hold signal is delivered from external to the chip.

5.2.2.2.16 Sample and Hold

The sample and hold comprises of a simple switch in series with the output of the final stage of shaping amplifier and a hold capacitor as shown in fig. 1. During normal operation, the switch is kept closed and the voltage across the hold capacitor tracks the output of the shaping amplifier, and when the hold signal is applied the signal across the capacitor is held.

5.2.2.2.17 Shaping Multiplexer

There is an on chip analog multiplexer that selects the output of either the LE or HE shaping amp outputs. This multiplexer is provided for testing of the circuits and is not required during flight.

5.2.2.2.18 Hold Multiplexer

There is an on chip analog multiplexer which selects the output of either the LE or HE Sample and Hold outputs, the output of this multiplexer is passed to the external ADC for digitization. The selection of the low or high-energy channel can be performed in the Auto mode or the manual mode. In the auto mode, an on chip discriminator on the output of LE shaping amp senses if the signal is near the saturation and switches the multiplexer to HE channel. In manual mode, the channel selection is under external control.

5.2.2.2.19 Auto Mode Channel Selection Comparator

A discriminator is provided at the output of low energy shaping amp and is set slightly below the upper saturation of the signal. When this discriminator fires, signaling a large signal, the Hold multiplexer automatically switches to the high energy channel when the ASIC is set to Auto mode.

5.2.2.2.20 Threshold Settings

On-chip DACs are provided to set the various baselines and thresholds as needed by various sub circuits and discriminators. The DACs are described in the next section.

5.2.2.2.21 Digital-to-Analog Converters (DACs)

5.2.2.2.21.1 Overview:

The DACs are used to set the discriminator threshold as follows:

Signal	Min Setting	Max Setting	Step Size	No. of Bits
Veto	0 MIP	3.2 MIPs	0.05 MIP	6 bits
LLD	0 MIP	3.2 MIP	0.05 MIP	6 bits
HLD	0 MIP	64 MIPs	1 MIP	6 bits

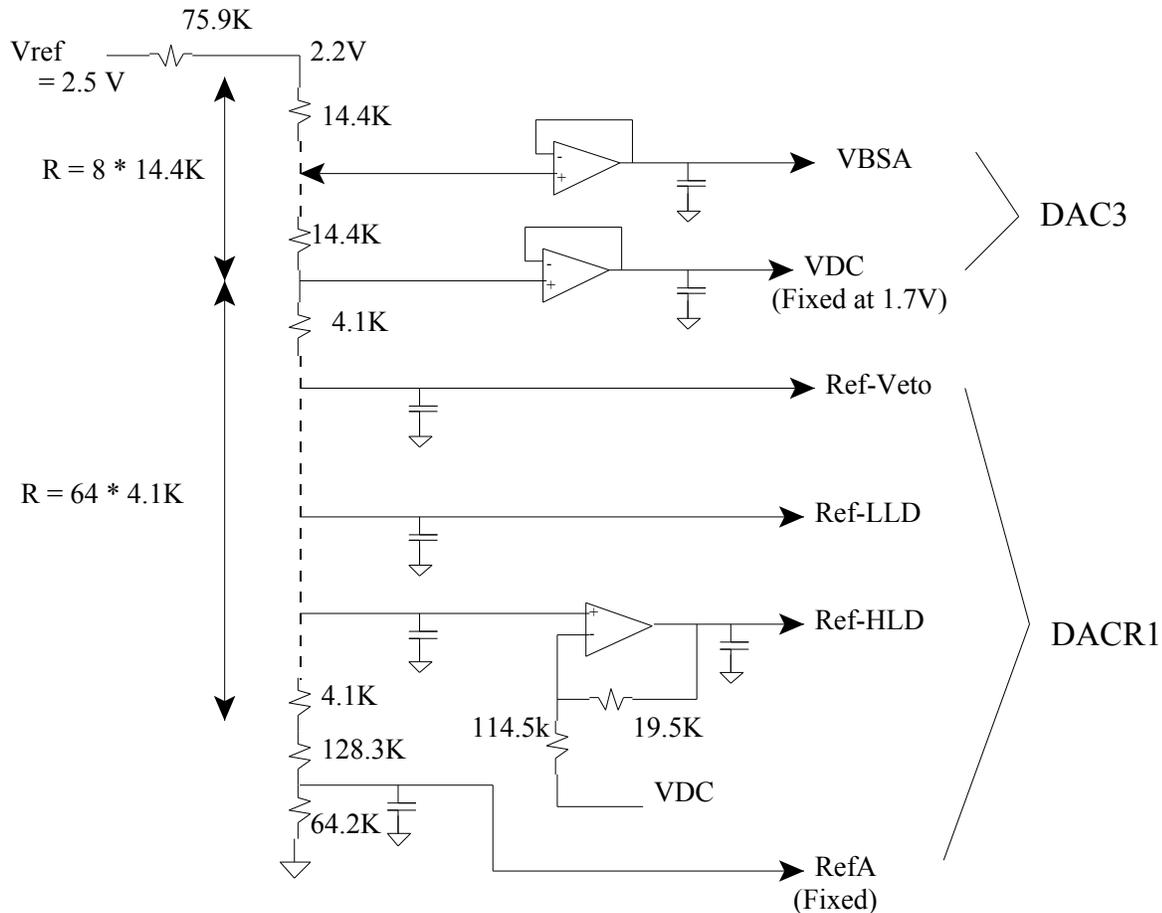
The Test Charge injection DAC is also a 6-bit DAC that sets the voltage level to the test charge injection between 0 and 2.5 Volt. The Base Line DAC is a 3-bit DAC that sets the baseline at the output of the Shaping Amps between 2.2 V and 1.75 V, the nominal setting is 2 V.

The DAC block also generates fixed voltages for the following:

- Disc Base Line level: This is set to 1.75 V, the signal going into all the discriminators have a dc offset of this value of 1.75 V. The signal going into the discriminators is an inverted exponential in shape, and therefore the various thresholds are set below this baseline.
- Auto Channel Select Discriminator Level: This is set to 0.8 V. When the signal in the low energy channel has exceeded the difference between this voltage and the DC base line at the shaping amp out, then the auto channel discriminator fires and this is used to switch the PHA to the high-energy channel.

5.2.2.2.21.2 The DAC architecture:

The DACs are implemented using a resistive divider chain as shown in the figure below. There are three DAC modules on the ASIC, DAC3 provides the level for the baseline at the output of the



An Overview of the DAC architecture in GAFE ASIC

Shaping amps and that at the input to the discriminators. DACR1 provides the threshold references for the discriminators. DACT provides the reference level for the on chip Test Charge injection circuit. As shown in figure ???, the DACs are formed using a resistive chain. DAC3 and DACR1 are in series with voltage reference which is set at 2.5 V. DACT is a separate chain of 64 resistors across V_{ref} and ground, the output of this DAC determines the level of on chip Test charge injection. The structure and functioning of the various DACs is described next.

5.2.2.2.21.3 DAC3: VBSA and VDC generation

The DAC3 is a 3-bit DAC that is formed by a series of 8 resistances each of 14.4K. This DAC is in series with a 75.9K resistor connected to the V_{ref} , which is set at 2.5V. The bottom end of the resistive chain is connected to the resistive chain for the 8-bit DACR1.

VBSA: The 3-bit DAC input is applied to a 3-bit to 8 line decoder module that selects one of the 8 nodes in the resistive chain. The output of this resistive chain is buffered and made available as VBSA, which is used to set the baseline at the output of shaping amps used for PHA. The nominal value of VBSA is 2 V. This level can be set between 1.7 V and 2.2 V using the 3-bit DAC.

VDC: This voltage is fixed to 1.7 V approximately and is made available from the bottom of the resistive chain comprising DAC3. This level determines the baseline at the input to the discriminators used to generate the various triggers.

5.2.2.2.21.4 DACR1: Threshold settings for Veto, LLD, HLD and PHA range select

This DAC comprises of 64 resistors in series. There are three 6-bit-to-64-line decoders to independently select the threshold for each of the Veto, LLD and HLD. The level for PHA range select is fixed. Since this DAC is in series with DAC3 or the bottom node of DAC3, which determines the VDC level, the threshold settings are always guaranteed to be relative to the baseline (VDC) and therefore any drift in the baseline is not going to affect the performance of the discriminators.

Veto & LLD: Veto and LLD thresholds are set able in 64 steps with 6-bit DACs. Since these thresholds are set to real low levels of the incoming signal, the signal from the PMT is first amplified by 20 before being fed to the Veto and LLD discriminators.

HLD: This sets the high-level discriminator threshold. This is a 6-bit DAC, which allows for 64 steps of settings.

Since the pulses are inverted, a signal of greater amplitude means setting the threshold farther below the baseline of VDC. The DAC setting of x3f or all "1"s, will set the threshold at the top or at VDC, which would actually mean a signal amplitude of zero. Conversely, a DAC setting of all "0"s would set the threshold at the bottom of the DAC which would correspond to full scale signal. Therefore the DAC bits should be set to x3f less the desired signal amplitude setting.

RefA: PHA range select threshold: This is a fixed voltage set near the full scale of the PHA. When the signal in the low energy channel PHA exceeds this threshold, the output of this discriminator is used to select the High energy channel for PHA. This level is presently set to 0.75 V.

5.2.2.2.21.5 DACT: Test Charge injection DAC

This DAC is also a 64 series resistor DAC strung across the Vref of 2.5 volts and ground. This 6-bit DAC determines the level of the test charge injection. An on chip capacitor of approximately 16 pF has been fabricated, for a 2.5 V input, this would allow charge injection of 40 pC or 62.5 MIPs.

5.2.2.2.22 GAFE Logic Module

The GAFE ASIC contains a digital module that controls the various functions of the ASIC. The digital interface is through a serial data bus, which comprises of a received data, return data and a clock. This serial link is implemented using low voltage differential signals; the chip is selected by an address ID for which there are 5 address pins available. The main function of the serial link is to program the various DACs, and set a few other parameters. The ASIC also outputs the various discriminator levels in a low voltage differential form, however to save on pins, the returns of some of the signals are tied together to form a common return. In addition, the digital module also selects the multiplexer channel to select either the high or low gain channel for PHA, controls the on chip test charge injection circuit, and operates the sample and hold.

5.2.2.2.22.1 Overview of the Logic Core

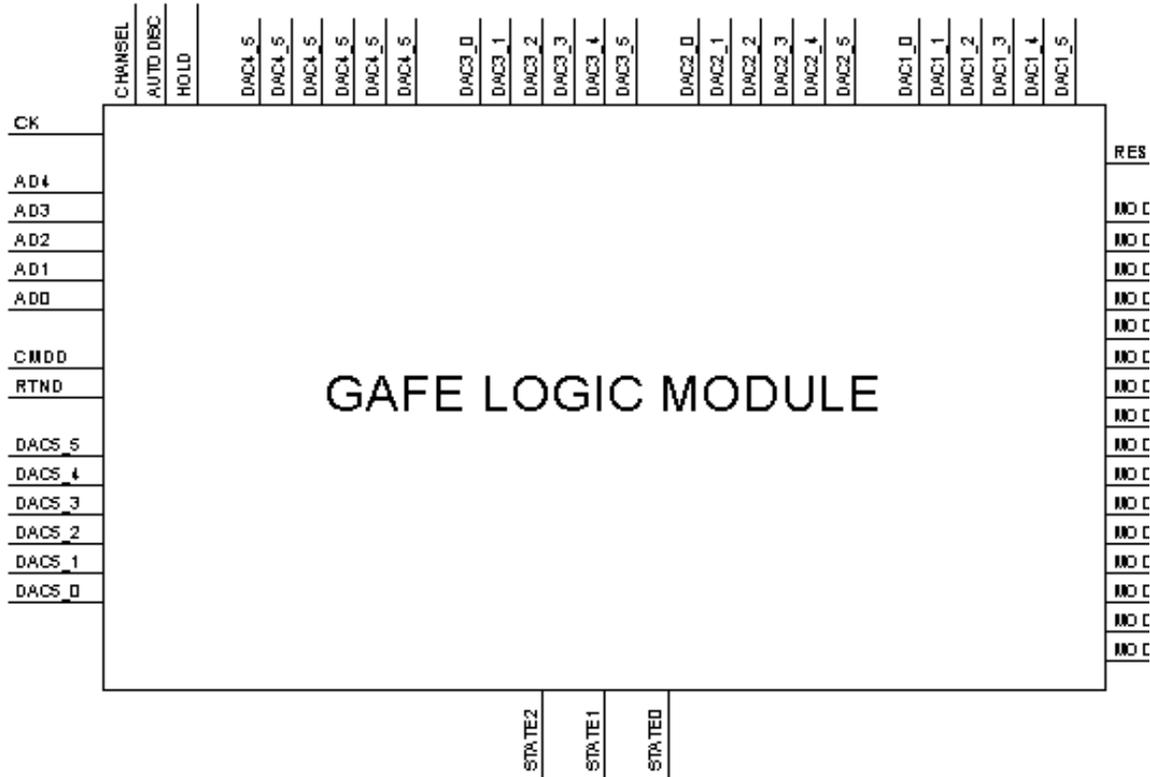
The design was done utilizing Verilog as the description language, Exemplar Leonardo Spectrum as the synthesis tool targeting the Tanner Agilent 0.5 μ m standard cell library, and Tanner L-Edit as the automated place and route layout tool. Core verification was performed via the Tanner LVS tool.

The GAFE logic has consists of a set of registers accessible via a command-response protocol. These registers may be written and read out by serial digital command. This serial data is GAFE_DAT and is clocked into the module on the positive going edge of GAFE_CLK.

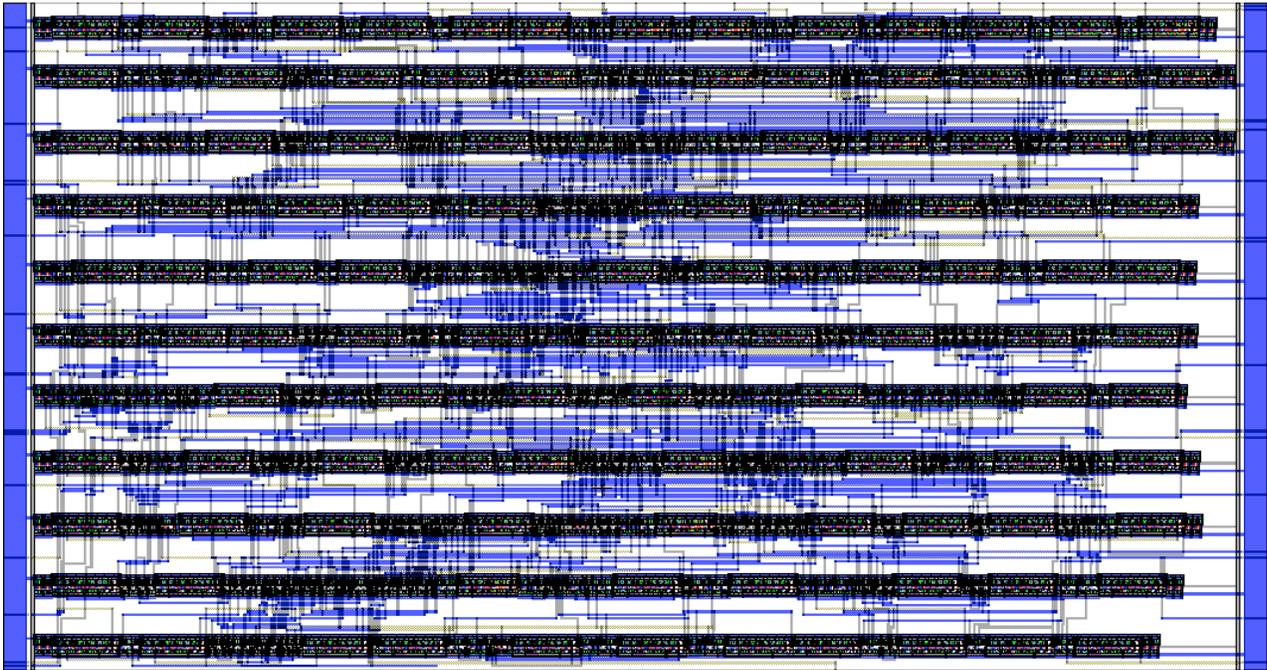
On a single FREE card, each GAFE has a unique address consisting of 5 voltage-level inputs, tied to either logic high or logic low through a series resistor. There is one 16-bit GAFE Mode register and five six bit DAC control registers (e.g., DAC1 – DAC5) available for configuration and are described below. There are five diagnostic commands available.

All GAFE commands originate in the LAT/AEM and pass through the GARC for formatting. Sufficient time is allowed by the GARC for one command to execute before the next GAFE command is sent. In the case of "Write" commands, this is at least 8 trailing zero bits. For "Read" commands, at least 28 trailing zero bits should be sent to allow for the full GAFE readback. This is controlled in the GARC by the garc_cmd_proc state machine.

A block diagram of the layout of the GAFE core logic module is shown below.



The physical layout of the GAFE logic core module is shown below.



5.2.2.22.2 GAFE Configuration Command Data Format:

The GAFE logic core responds only to properly structured commands. This format is detailed in the table below.

Bit(s)	Bit Description	Value
27	Start Bit	1
26	Read/Write Bit	0 = Write, 1 = Read
25:21	GAFE Chip Address	Hardwired inputs. Value 'h1F is reserved for broadcast write commands. Nominal values are 0 – 17 on FREE PCB.
20:17	GAFE Register Select	0: GAFE Mode Register[15:0] (read/write) 1: DAC_1 [5:0] (read/write) 2: DAC_2 [5:0] (read/write) 3: DAC_3 [5:0] (read/write) 4: DAC_4 [5:0] (read/write) 5: DAC_5 [5:0] (read/write) 6: Version (diagnostic: read-only) 7: Write Counter (diagnostic: read-only) 8: Reject Counter (diagnostic: read-only) 9: Loop Counter (diagnostic: read-only) 10: Chip Address (diagnostic: read-only)
16:1	GAFE Config Data	
0	Parity Bit	Odd parity over [26:1]

5.2.2.2.22.3 Contents of the GAFE Mode Register

The GAFE core contains one 16-bit register to be used for the static configuration of multiple modes. These bits are utilized in version 2 of the GAFE as detailed in the table below.

GAFE Mode Bit(s)	Description	"0" State	"1" State	Default
0	TCI Gain	Lo	Hi	0
1	TCI Pulse Enable	Disable	Enable	1
2	Autorange Select	Auto	Manual	0
3	Range Select	Lo	Hi	0
4	VETO Disc Enable	Disable	Enable	1
5	HLD Disc Enable	Disable	Enable	1
15:6	Spare Mode Bits	--	--	0

5.2.2.2.22.4 Description of the Diagnostic Readback Registers

Reading back register 6 provides the GAFE hardware version number in return data. For the May 2002 submission (GAFE_2), this number is 2. Reading back register 7 provides a count of the number of valid configuration commands written to the register. This is initially reset to 0 and rolls over at a count value of 63. Reading back register 8 provides a count of rejected commands since power up. This counter rolls over at 63. Reading back register number 9 provides a counter of the number of times the state machine loop has completed, also rolling over at 63. Register number 10 provides a readback of the hard-wired chip address.

5.2.2.2.22.5 GAFE Return Data Format:

The GAFE core returns configuration data when a valid readback command is received. The return data format is basic and listed in the table below.

Bit(s)	Bit Description	Value
16	Start Bit	1
15:0	GAFE Configuration Return Data	Mode register is 16 bits in length Other registers are padded with leading zeroes in the most significant bits.

5.2.2.2.22.6 GAFE Commands

The following table represents each of the available GAFE commands. In this table, **a** is the 5 bit hexadecimal chip address, **dddd** is the 16 bit hexadecimal data word, and **p** is the odd data parity. Note that a GAFE will process a write command either for the address hard-wired to the chip address pins or to an address of 'h1F'. A GAFE will process a read command only for an address identical to the hard-wired address. It is an operational constraint that, for any given ACD circuit board, each GAFE must have a unique address.

	GAFE Command Mnemonic	Command Pattern	Command Function
1	GAFE_Mode_Write	1 0 a 0000 dddd p	Write to the GAFE Mode Register
2	GAFE_DAC1_Write	1 0 a 0001 00dd p	Write to the GAFE DAC #1 Register
3	GAFE_DAC2_Write	1 0 a 0010 00dd p	Write to the GAFE DAC #2 Register
4	GAFE_DAC3_Write	1 0 a 0011 00dd p	Write to the GAFE DAC #3 Register
5	GAFE_DAC4_Write	1 0 a 0100 00dd p	Write to the GAFE DAC #4 Register
6	GAFE_DAC5_Write	1 0 a 0101 00dd p	Write to the GAFE DAC #5 Register

7	GAFE_Mode_Read	1 1 a 0000 0000 1	Read from the GAFE Mode Register
8	GAFE_DAC1_Read	1 1 a 0001 0000 1	Read from the GAFE DAC #1 Register
9	GAFE_DAC2_Read	1 1 a 0010 0000 1	Read from the GAFE DAC #2 Register
10	GAFE_DAC3_Read	1 1 a 0011 0000 1	Read from the GAFE DAC #3 Register
11	GAFE_DAC4_Read	1 1 a 0100 0000 1	Read from the GAFE DAC #4 Register
12	GAFE_DAC5_Read	1 1 a 0101 0000 1	Read from the GAFE DAC #5 Register
13	GAFE_Version	1 1 a 0110 0000 1	Read back the GAFE logic version
14	GAFE_Write_Ctr	1 1 a 0111 0000 1	Read back the GAFE Write Counter (diagnostic)
15	GAFE_Reject_Ctr	1 1 a 1000 0000 1	Read back the GAFE Cmd Rejects Counter (diagnostic)
16	GAFE_Cmd_Ctr	1 1 a 1001 0000 1	Read back the GAFE Total Commands Counter (diagnostic)
17	GAFE_Chip_Addr	1 1 a 1010 0000 1	Read back the GAFE Chip Address (diagnostic)

5.2.2.2.22.7 Auto-Discriminator Logic

An independent logic module is contained in the GAFE core. This is used to control the position of the shaping amplifier selection multiplexer. This logic is clocked by the positive edge of the HOLD signal. The values of the AUTODISC discriminator and GAFE Mode bits 2 and 3 are used to determine the control of the multiplexer to select either the low energy (LE) or the high energy (HE) channels. This flip-flop and control logic will be tested with the analog portion of the GAFE.

The channel selection indicator, the CHID pin, is not returned in the serial return data. Verification of this function will be performed with an oscilloscope in the analog verification procedure of the GAFE.

The logic for the multiplexer channel selection is as follows:

AUTODISC	Mode[2]	Mode[3]	Channel Select	Description
0	0	0	0	Auto, Lo
0	0	1	0	Auto, Hi
0	1	0	0	Manual, Lo
0	1	1	1	Manual, Hi
1	0	0	1	Auto, Lo
1	0	1	1	Auto, Hi
1	1	0	0	Manual, Lo
1	1	1	1	Manual, Hi

5.2.2.2.23 Pin Out

The various pins of the ASIC are described next. The ASIC has 48 bonding pads, the pin numbering starts from the top left and goes anticlockwise.

5.2.2.2.23.1 Supply Pins:

VCC: Pins: 1, 11: Analog Power, 3.3 V. These pins should have a 0.1 uf cap very close to the ASIC on the board the chip is mounted. If there is only enough space available for one 0.1 uf cap on the board, then it should be mounted close to pin 1.

Agnd: Pins: 2, 4, 6, 8, 12, 33, 35: Analog ground.

Vdd: Pins: 24, 38: Digital Power, 3.3V. These pins should have a 0.1 uf cap very close to the ASIC on the board the chip is mounted. If there is only enough space available for one 0.1 uf cap on the board, then it should be mounted close to pin 24

Dgnd: Pins: 13, 37,47. Digital ground.

5.2.2.2.23.2 Analog Pins:

salo: Pin 3: Slow Amp, Low Energy Input: This is the input for the low energy or high gain channel for the PHA. To this input, a 12K (R1) resistor is connected as shown in Fig.1. This resistor in conjunction with the R2 connected to sahi, splits the charge into two channels for PHA.

sahi: Pin 5: Slow Amp, High Energy Input: This is the input for the high energy or low gain channel for the PHA. To this input, a 1200K (R2) resistor is connected as shown in Fig.1. This resistor in conjunction with the R1 connected to salo, splits the charge into two channels for PHA.

discin: Pin 7: Input to the Fast channel for discriminators: To this a 12 K (R3) is connected as shown in Fig.1. This is a high impedance input to a fast shaping or large bandwidth amp. The output of this amp is to generate triggers for Veto and LLD.

Vref: Pin 9: 2.5 V Reference. This pin should be bypassed with a 0.1uf cap close to the ASIC. This is the reference input which is used by the DACs to generate the various discriminator thresholds and also is used to set the baseline for the shaping amps and of the signal that is input to the discriminators.

muxh: Pin 34: Multiplexer out for the Sampl and Hold outputs of the low and high energy PHA channels. This pin is connected to the ADC input.

muxsa: Pin 36: Multiplexer out for the shaping amp. This is the multiplexed shaping amp out for the low and high energy channels. This output is only meant for testing and diagnosis, it is not to be used on the final flight board.

tci: Pin 48: Test charge injection output. This is the charge injection output which is applied to the node where the two charge splitting resistances R1 and R2 meet, the connection to this node is via a 3k resistance is added as shown in Fig.1.

sparea: Pin 10: This is a spare pin associated with the analog modules.

5.2.2.2.23.3 The Digital Pins:

a0, a1, a2, a3, a4: Pns: 30, 31, 32, 44, 45 respectively: Address Pins: These pins are tied either to ground or to Vdd and determine the address or the ID of the ASIC.

LLD: Pin 29: This is the ZS or LLD out, this is a low voltage differential signal, but its return is in common with the Veto and Chnid. Having a common return, saves 2 pins per GAFE ASIC, and since there are 18 GAFE ASICs connected to one GARC ASIC, this results in a saving of 36 pins on the GARC.

VETO: Pin 28: This is the VETO out, this is a low voltage differential signal, but its return is in common with the LLD and Chnid. Having a common return, saves 2 pins per GAFE ASIC, and since there are 18 GAFE ASICs connected to one GARC ASIC, this results in a saving of 36 pins on the GARC.

chnid: Pin 27: A high indicates that high energy PHA channel has been selected for the multiplexed outputs. This is a low voltage differential signal, but its return is in common with the Veto and LLD. Having

a common return, saves 2 pins per GAFE ASIC, and since there are 18 GAFE ASICs connected to one GARC ASIC, this results in a saving of 36 pins on the GARC.

irtn: Pin 26: This is the common return pin for signals LLD, VETO and chnid.

HLD2 and HLD1: Pins 18 and 19 respectively. This is a pseudo-differential out of the High level discriminator. Across these two pins is switch, which is turned on when the discriminator is fired, otherwise it is off. The HLDs from all the GAFE ASICs are tied together to implement an “OR” gate. When the HLD on any one of the 18 GAFE ASICs fires, the impedance between the HLD2 and HLD1 is lowered, and this is sensed by the GARC chip.

reset: Pin 25: This is the reset pin for digital logic.

Hold+ and Hold- : Pins 23 and 22 respectively: These are the differential hold inputs which make the PHA sample and hold circuit to switch from tracking to Hold mode

Strob+ and Strob- : Pins 21 and 20 respectively: These are differential strobe inputs, the signal which cause the charge injection of the on chip test pulser.

cmd+ and cmd- : Pins 41 and 42 respectively: These are low voltage differential inputs for the command data to the digital control module on the ASIC.

cmdck+ and cmdck- : Pins 39 and 40 respectively. These are low voltage differential inputs for the command clock to the digital control module on the ASIC.

rtnd: Pin 14: This is the return data from the digital block of GAFE ASIC.

state0, state1, state2: Pins 17, 16 and 15 respectively: These are the test outputs from the digital section of the GAFE ASIC and are meant for diagnosis only.

spared0 and spared1: Pins 43 and 46 respectively: These are spare pins associated with the digital modules of the GAFE ASIC.

5.2.2.2.24 Interfacing Issues:

5.2.2.2.24.1 Veto stretching:

The veto coming out of the ASIC should be stretched by 0.2 μ s before it is passed on to the LAT, this allows 0.2 μ s for the comparator to recover and be in a ready state to fire again if another signal arrived on the trailing edge of the stretched veto pulse. Assuming that the FPGA or the digital logic outside the ASIC can retrigger instantly after the trailing edge, the dead time of the ACD electronics is now effectively zero seconds. However, since the electronics has finite rise, fall and delay times, there will be some finite time of dead time which will be unavoidable.

5.2.2.2.24.2 Hold Signal:

The latency of the sample and hold from the LAT is 2 μ s, therefore, the minimum peaking time of the shaped pulse is 2 μ s. However, since the resistor and caps fabricated in silicon can vary by 20% from one run to another, the peaking time should be increased to $2 \mu\text{s}/0.8/0.8 = 3.125 \mu\text{s}$. A peaking time of 3 μ s has been chosen as the hold signal coming a little before the peak will not affect the linearity, but only reduce the gain slightly.

Therefore to sample the shaped signal at its peak value, the L1T trigger from the LAT should be delayed by 1us before sending it to the analog ACD ASIC. However, if the resistances and capacitors fabricated reveal that the actual value fabricated is 20% less than the designed, then the peaking time will occur at 2 us instead of 3us. For such cases the delay in the L1T trigger before it is applied as Hold signal to the

analog ASIC should be zero. Conversely, if the resistance and capacitance values fabricated are 20% over, then the peaking will occur at 4.7 μ s. In this case, the L1T trigger should be delayed by 4.7 - 2 = 2.7 μ s before it is applied as a hold signal to the analog ASIC.

Thus there should be an adjustable delay in series with the Hold signal going into the analog ASIC, this delay should be adjustable from 0 to 2.7 μ s.

5.2.2.2.25 Test Charge Injection

An on-chip test charge injection circuit will be included in the analog ASIC. The charge injection capacitor (internal to the analog ASIC) will have a value of approximately 16 pF. This will provide the following voltage-to-charge-to-MIP equivalence (for a nominal HLD threshold signal):

$$25 \text{ MIP} \Rightarrow (25)(10 \text{ pe}^-)(1.6022 \times 10^{-19})(400,000) = Q = 16 \text{ pC}$$

The charge injection circuit will be used for both aliveness tests and characterization of the FREE circuit card. The charge injection mode will be controlled via two mode bits, commandable from the FREE circuit card. The modes are described as follows:

CI Mode Bit 1	CI Mode Bit 0	Function
0	0	disabled
0	1	disabled
1	0	LO range enabled
1	1	HLD range enabled

Test Charge Injection Control Table

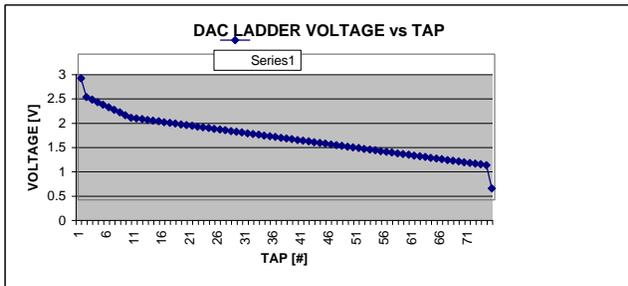
5.2.2.3 The charge injection circuit will have adjustable amplitude based on a 6-bit DAC voltage. This DAC is internal to the analog ASIC. The nominal rate of charge injection will be 1000 Hz when the circuit is enabled. In addition, the ACD electronics shall be capable of generating synchronous charge injection signals in response to broadcast commands from the AEM. Analog-to-Digital Converter

The ACD will utilize a commercially available MAXIM MAX145 analog-to-digital converter that is suitably qualified and screened. This part will be identical to the ADCs used on CAL and TKR, and will be provided to GSFC by SLAC.

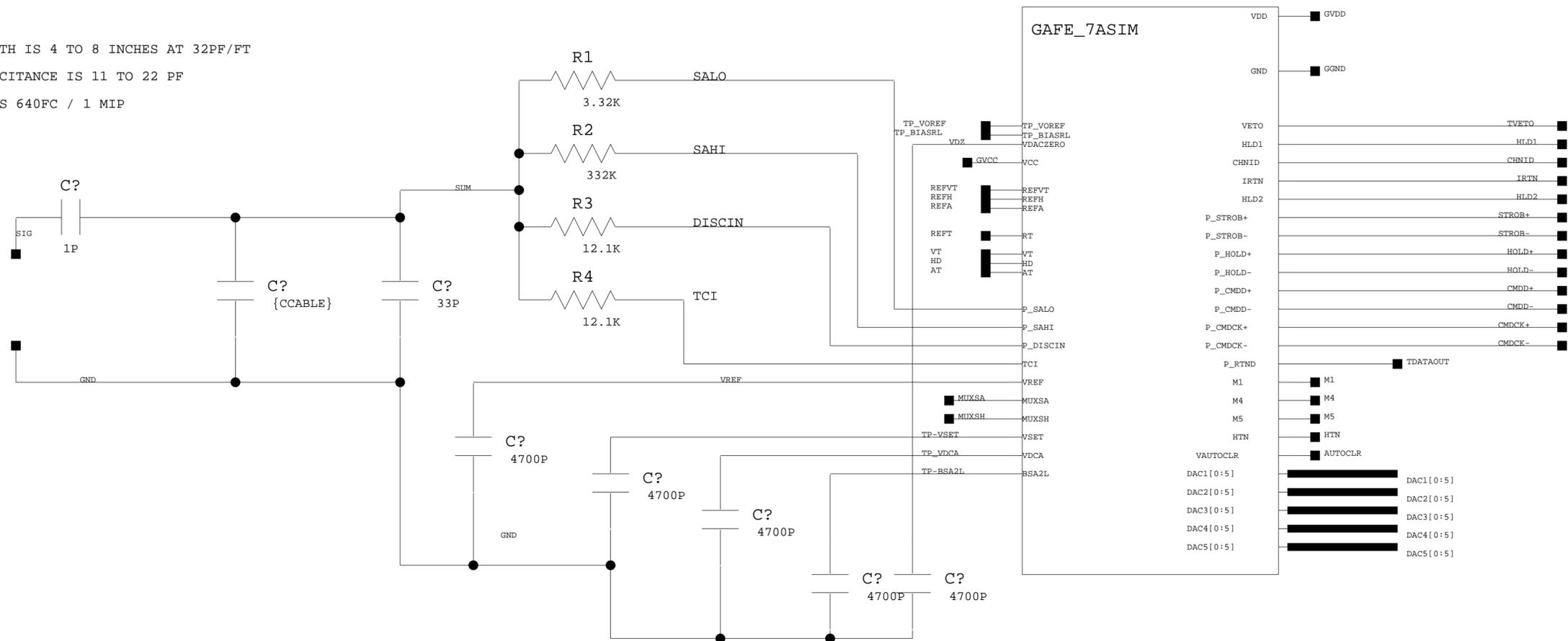
5.2.2.3.1 Spectral Performance of the Analog to Digital Converter

The analog-to-digital converter shall have a serial interface, operate from a single +3.3V supply, dissipate less than 10 mW at 1 kHz, and be in a surface-mount plastic package. It will be identical to that used on the CAL and TKR subsystems. This part will be supplied to GSFC by SLAC. The analog-to-digital converter will have a resolution of at least 11 bits. The signal-to-noise ratio of the analog system shall be a minimum of 66 dB. The analog-to-digital converter will be activated by the FREE circuit card logic whenever the LLD fires, the signal chain is not busy from a previous event, and L1T is received from the AEM. The analog-to-digital conversion time shall be less than 10 μ s. The low energy range will be digitized for pulses that are below the threshold range-switching discriminator. The high energy range will be digitized for pulses that are above the that threshold. There will be a test mode in which both ranges will be digitized, for cross-calibration.

Parameter	Value	OREF	BASELINE	00	1	0.00E+00	1311	0	1	2.5
VREF	2.5	1.2	01	1	200	1311	0	1	2.5	
RT	150		2.577918	02	1	28	1111	200	0.847445	2.118612
URD3	28	224	2.497826	03	2	28	1083	228	0.826087	2.065217
NRD3	8		2.417735	04	3	28	1055	256	0.804729	2.011823
NRD1	8		2.337643	05	4	28	1027	284	0.783371	1.958429
URD1	8	512	2.257551	06	5	28	999	312	0.762014	1.905034
NRD1	64		2.17746	07	6	28	971	340	0.740656	1.85164
RA1	250	375	2.097368	08	7	28	943	368	0.719298	1.798246
RA2	125		2.017277	09	8	28	915	396	0.697941	1.744851
CCAL0	3	1261	0A	1	8	887	424	424	0.676583	1.691457
GAIN	100		0B	2	8	879	432	432	0.670481	1.676201
PC/MIP	0.64		0C	3	8	871	440	440	0.664378	1.660946
			0D	4	8	863	448	448	0.658276	1.64569
			0E	5	8	855	456	456	0.652174	1.630435
			0F	6	8	847	464	464	0.646072	1.615179
CCAL0	16.35		10	7	8	839	472	472	0.639969	1.599924
GAIN	1		11	8	8	831	480	480	0.633867	1.584668
PC/MIP	0.64		12	9	8	823	488	488	0.627765	1.569413
			13	10	8	815	496	496	0.621663	1.554157
			14	11	8	807	504	504	0.615561	1.538902
			15	12	8	799	512	512	0.609458	1.523646
G_LS			16	13	8	791	520	520	0.603356	1.508391
			17	14	8	783	528	528	0.597254	1.493135
			18	15	8	775	536	536	0.591152	1.477879
			19	16	8	767	544	544	0.58505	1.462624
			1A	17	8	759	552	552	0.578947	1.447368
			1B	18	8	751	560	560	0.572845	1.432113
			1C	19	8	743	568	568	0.566743	1.416857
			1D	20	8	735	576	576	0.560641	1.401602
			1E	21	8	727	584	584	0.554539	1.386346
			1F	22	8	719	592	592	0.548436	1.371091
			20	23	8	711	600	600	0.542334	1.355835
			21	24	8	703	608	608	0.536232	1.34058
			22	25	8	695	616	616	0.53013	1.325324
			23	26	8	687	624	624	0.524027	1.310069
			24	27	8	679	632	632	0.517925	1.294813
			25	28	8	671	640	640	0.511823	1.279558
			26	29	8	663	648	648	0.505721	1.264302
			27	30	8	655	656	656	0.499619	1.249047
			28	31	8	647	664	664	0.493516	1.233791
			29	32	8	639	672	672	0.487414	1.218535
			2A	33	8	631	680	680	0.481312	1.20328
			2B	34	8	623	688	688	0.47521	1.188024
			2C	35	8	615	696	696	0.469108	1.172769
			2D	36	8	607	704	704	0.463005	1.157513
			2E	37	8	599	712	712	0.456903	1.142258
			2F	38	8	591	720	720	0.450801	1.127002
			30	39	8	583	728	728	0.444699	1.111747
			31	40	8	575	736	736	0.438596	1.096491
			32	41	8	567	744	744	0.432494	1.081236
			33	42	8	559	752	752	0.426392	1.06598
			34	43	8	551	760	760	0.42029	1.050725
			35	44	8	543	768	768	0.414188	1.035469
			36	45	8	535	776	776	0.408085	1.020214
			37	46	8	527	784	784	0.401983	1.004958
			38	47	8	519	792	792	0.395881	0.989703
			39	48	8	511	800	800	0.389779	0.974447
			3A	49	8	503	808	808	0.383677	0.959191
			3B	50	8	495	816	816	0.377574	0.943936
			3C	51	8	487	824	824	0.371472	0.92868
			3D	52	8	479	832	832	0.36537	0.913425
			3E	53	8	471	840	840	0.359268	0.898169
			3F	54	8	463	848	848	0.353166	0.882914
				55	8	455	856	856	0.347063	0.867658
				56	8	447	864	864	0.340961	0.852403
				57	8	439	872	872	0.334859	0.837147
				58	8	431	880	880	0.328757	0.821892
				59	8	423	888	888	0.322654	0.806636
				60	8	415	896	896	0.316552	0.791381
				61	8	407	904	904	0.31045	0.776125
				62	8	399	912	912	0.304348	0.76087
				63	8	391	920	920	0.298246	0.745614
				64	8	383	928	928	0.292143	0.730359
				1	250	375	936	936	0.286041	0.715103
				1	125	125	1186	1186	0.095347	0.238368
						1311				



CABLE LENGTH IS 4 TO 8 INCHES AT 32PF/FT
 CABLE CAPACITANCE IS 11 TO 22 PF
 PMT GAIN IS 640FC / 1 MIP



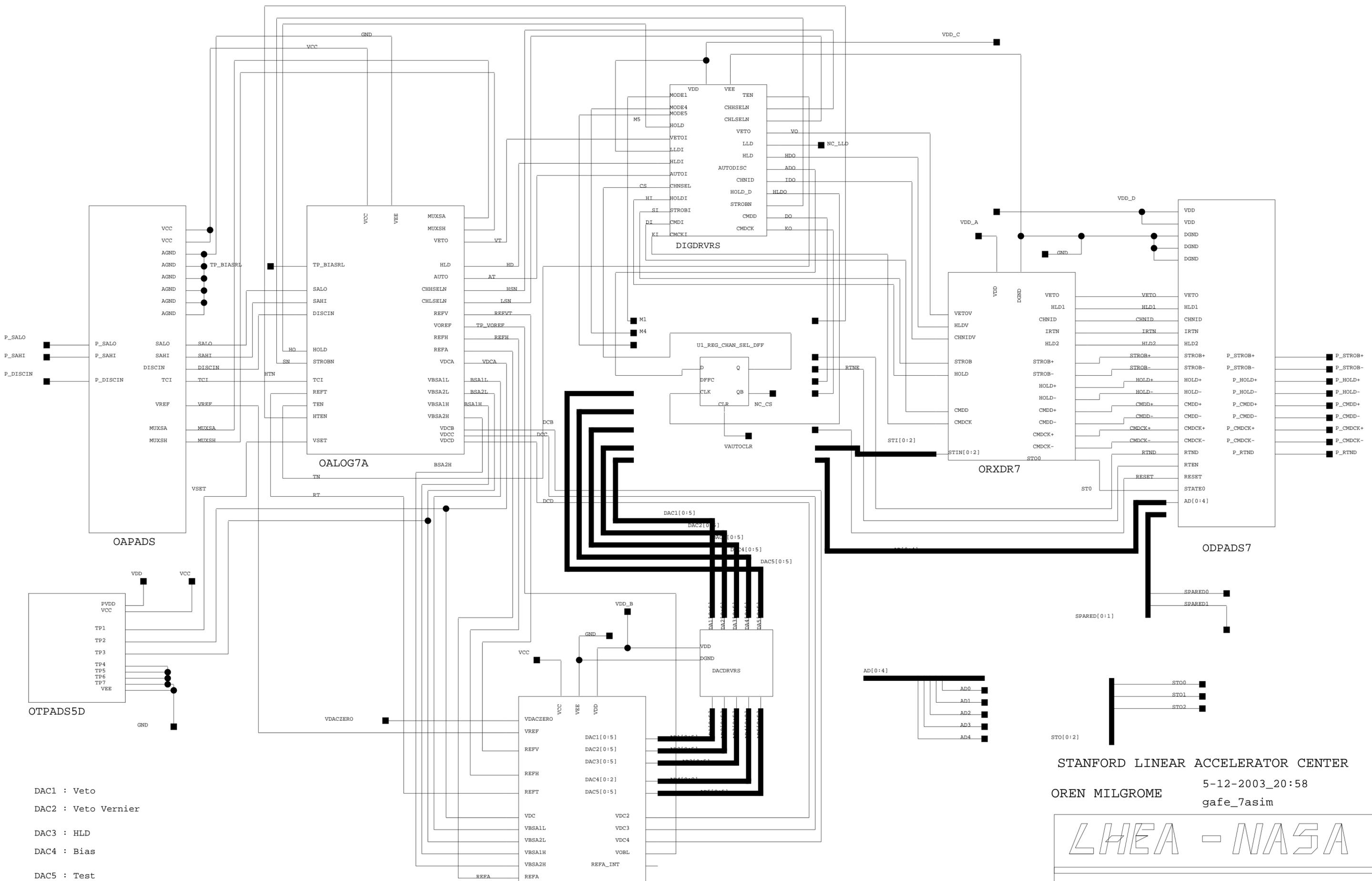
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gafe7a_testbench

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DAC1 : Veto
 DAC2 : Veto Vernier
 DAC3 : HLD
 DAC4 : Bias
 DAC5 : Test

MODE0 : HIGH ENERGY DISCRIMINATOR ENABLE
 MODE1 : LOW RANGE CAL ENABLE
 MODE4 : VETO DISCRIMINATOR ENABLE
 MODE5 : HIGH RANGE CAL ENABLE

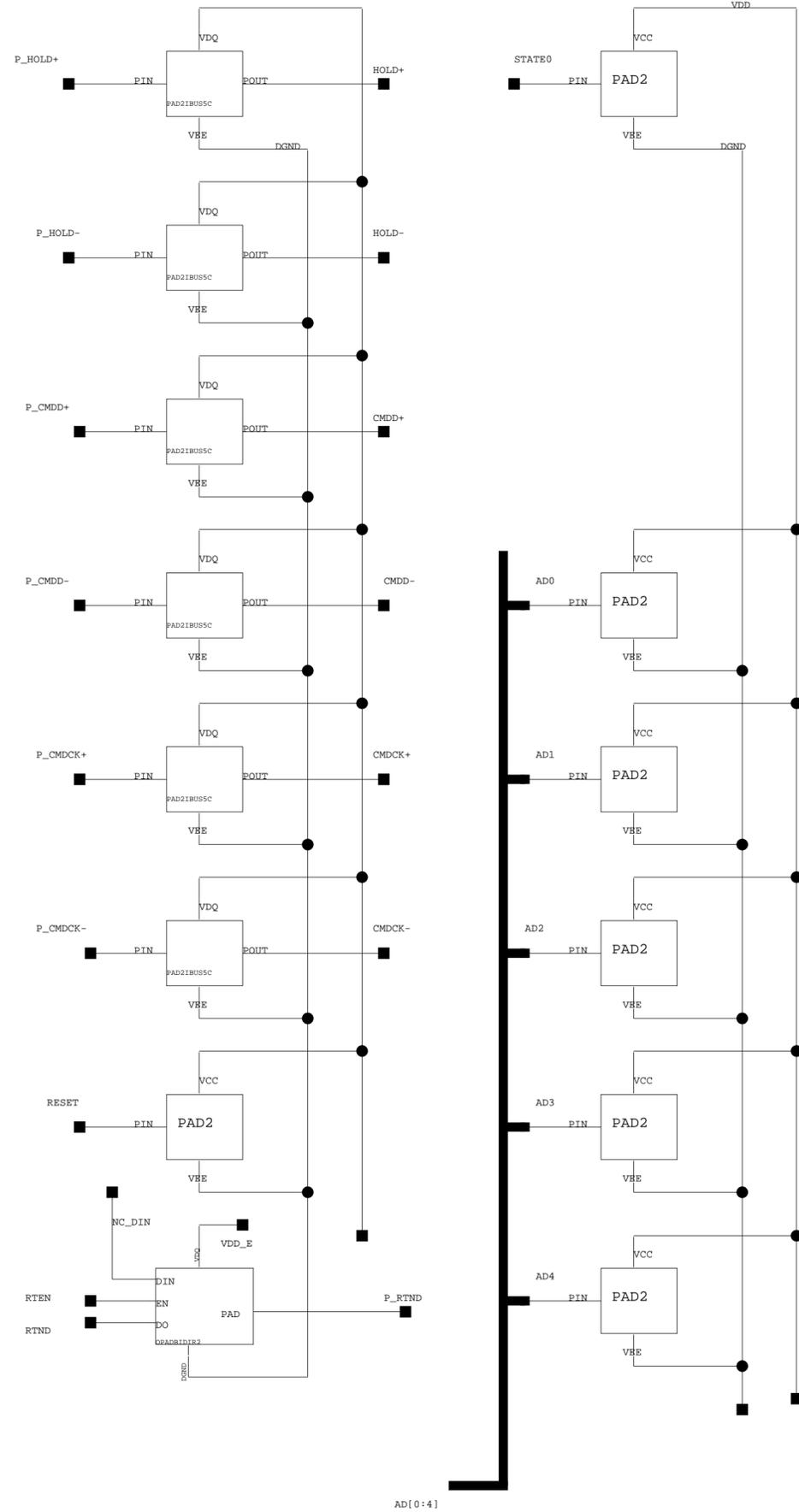
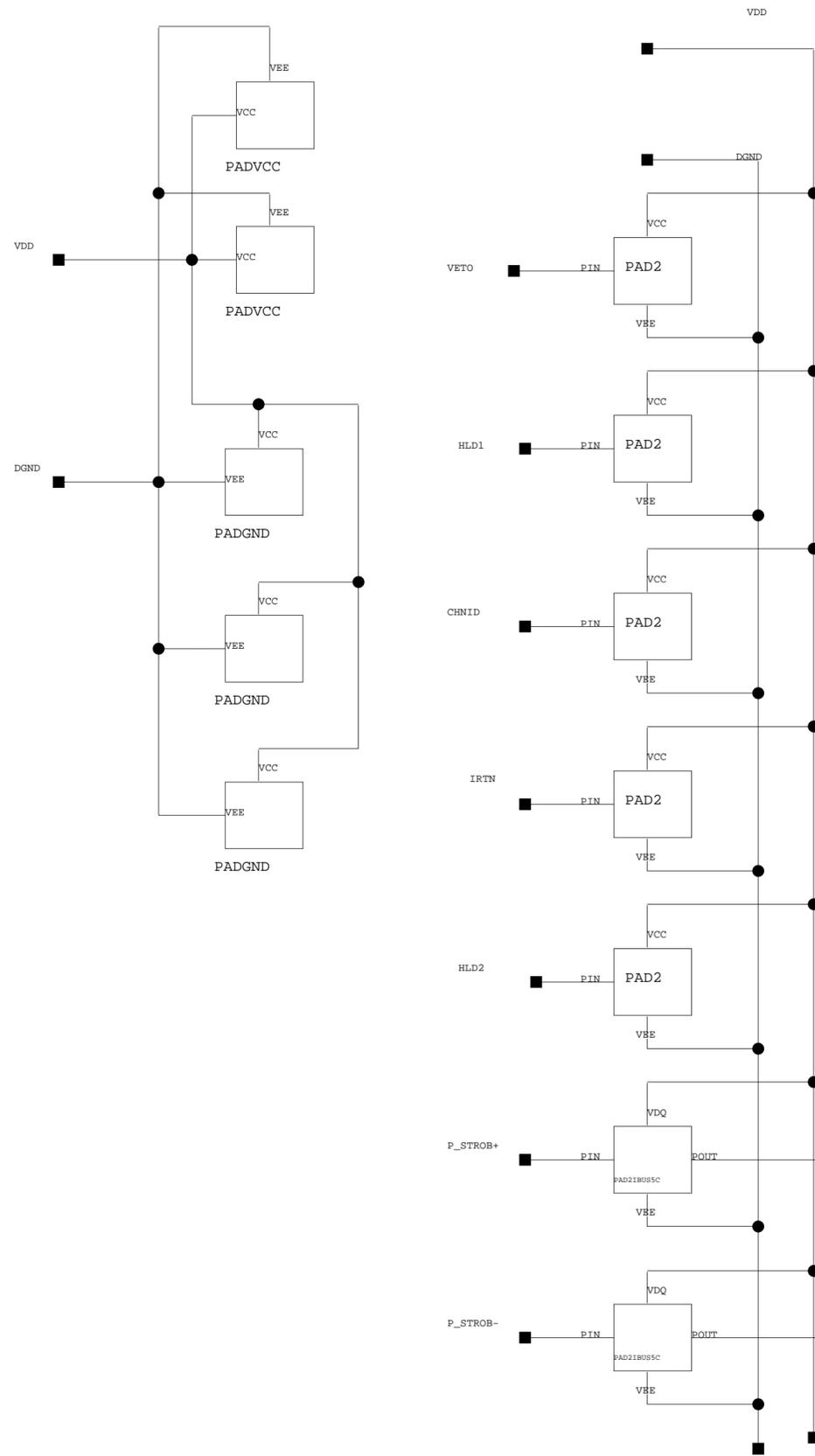
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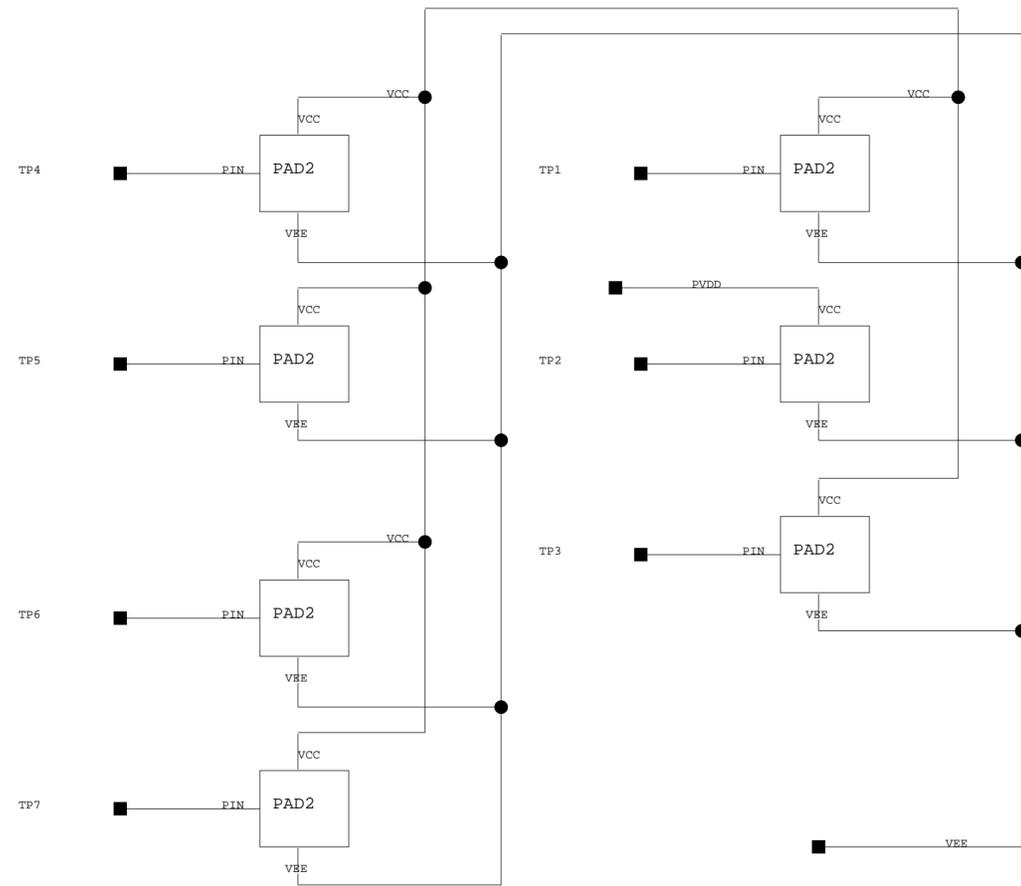
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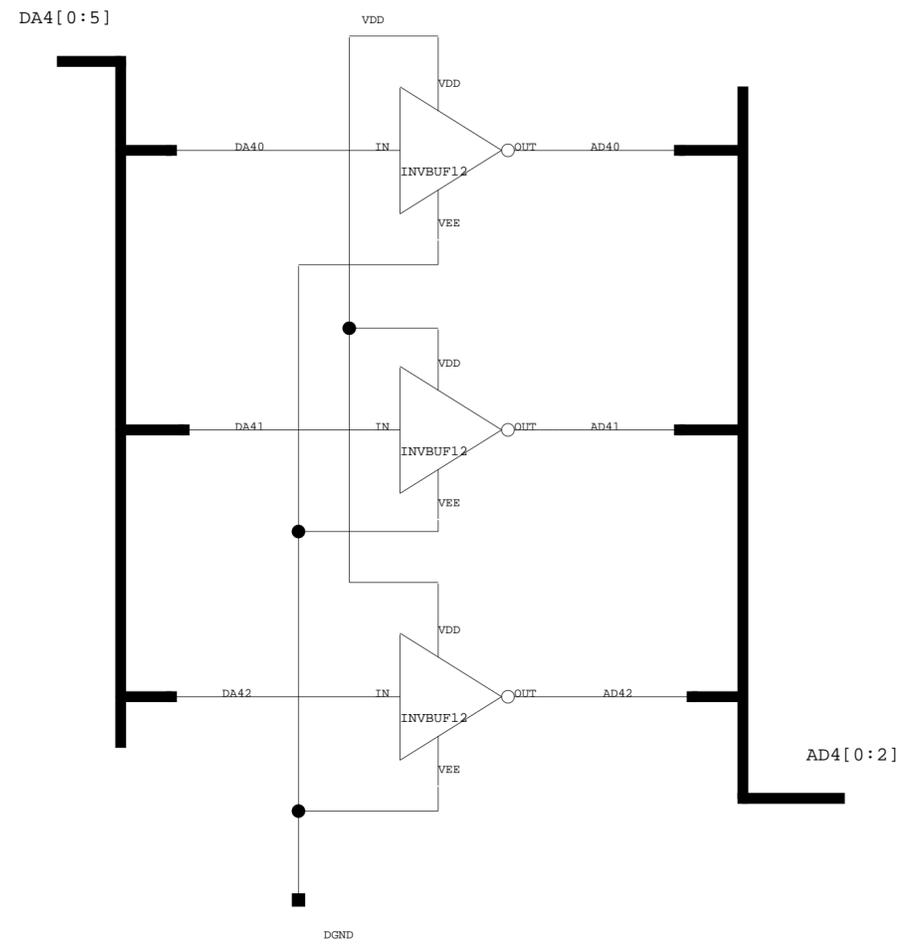
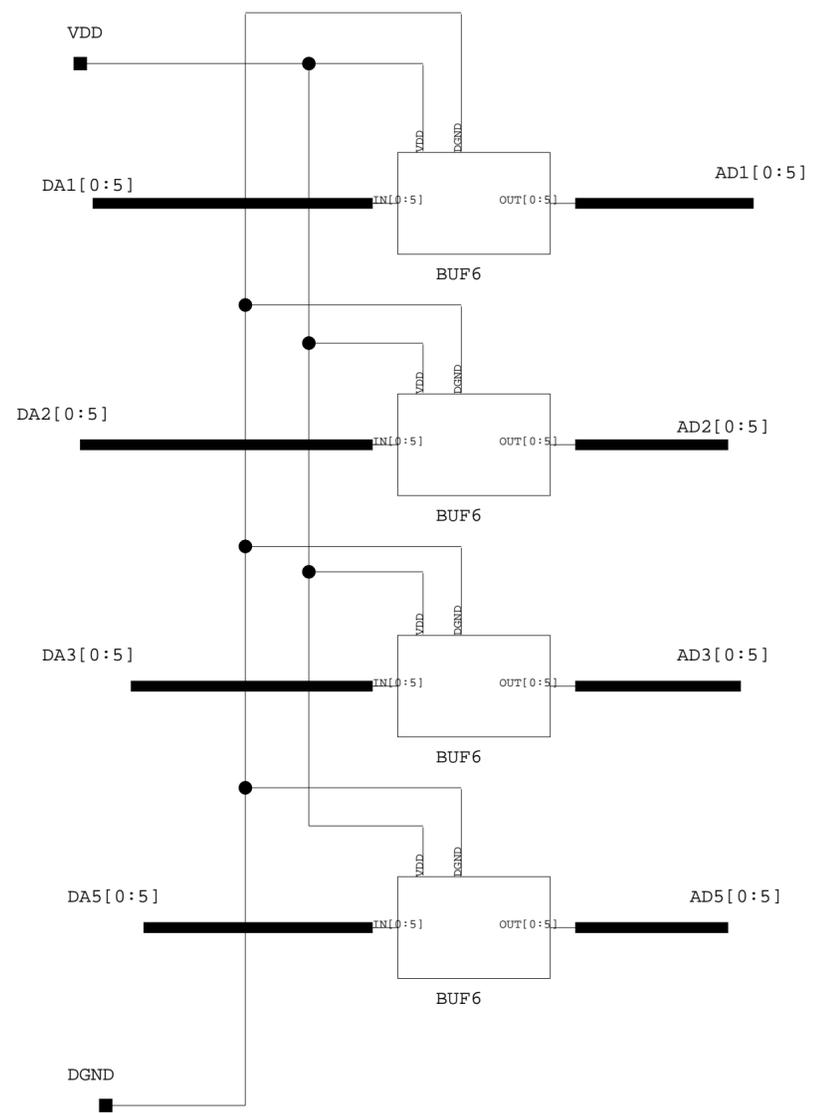
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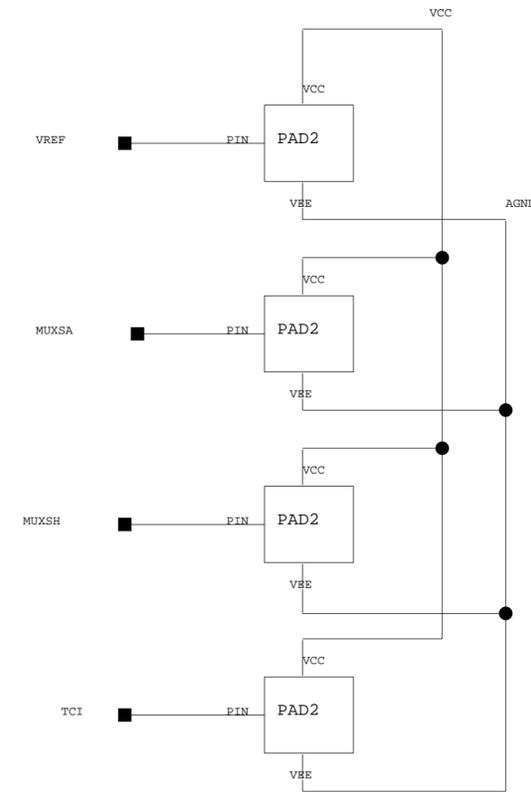
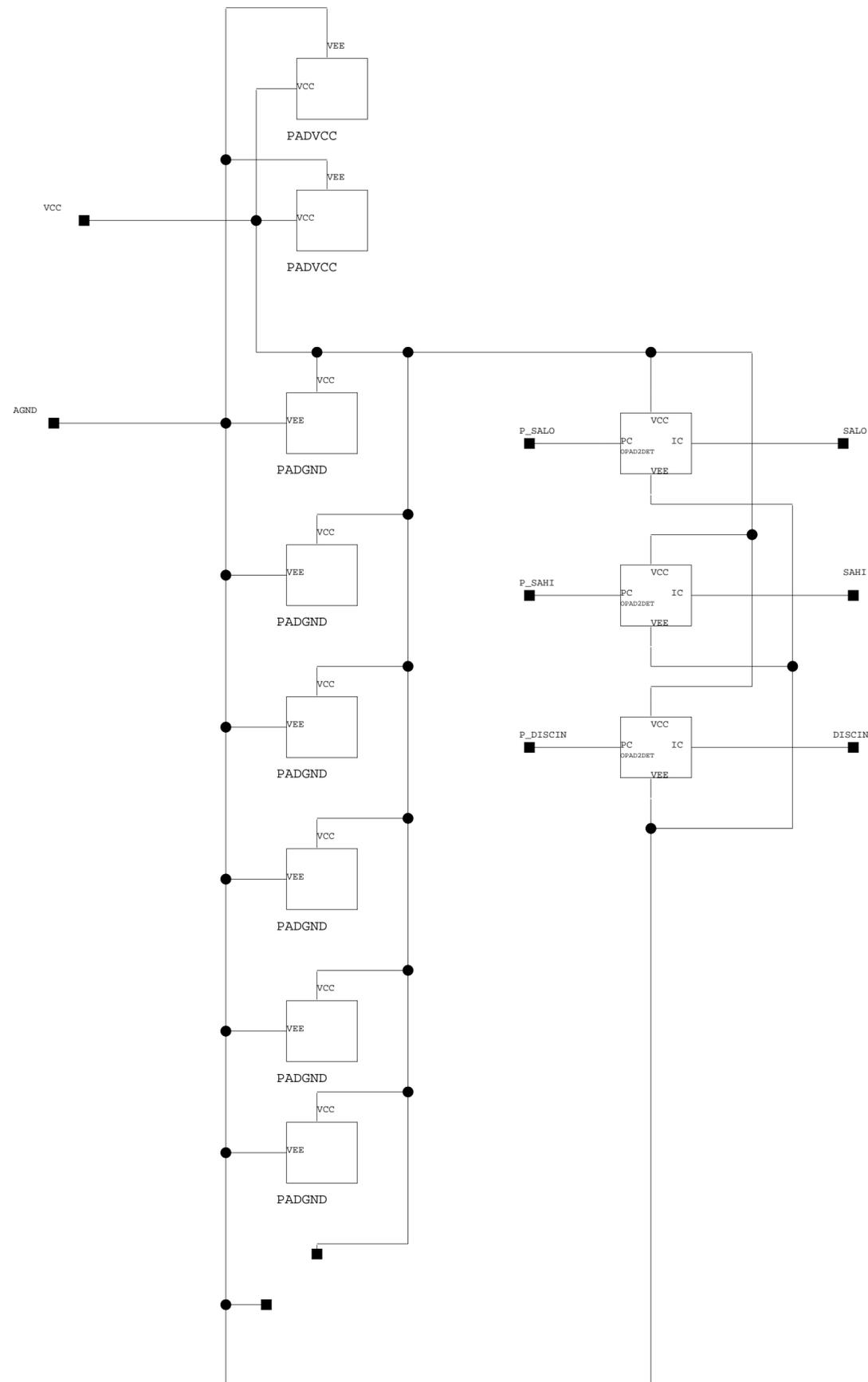
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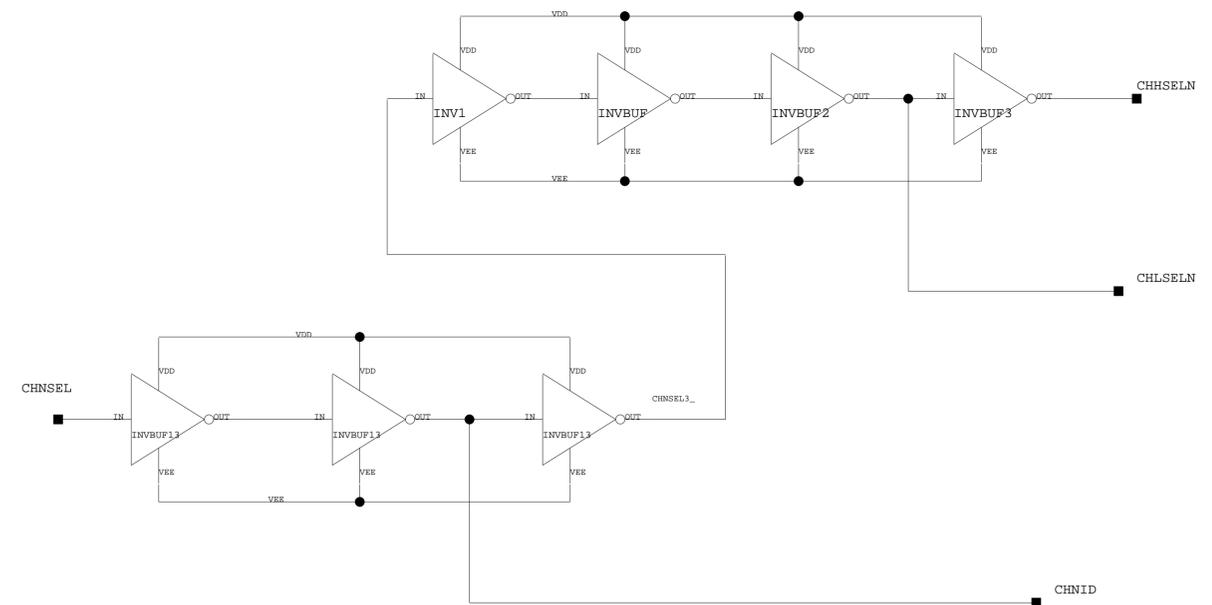
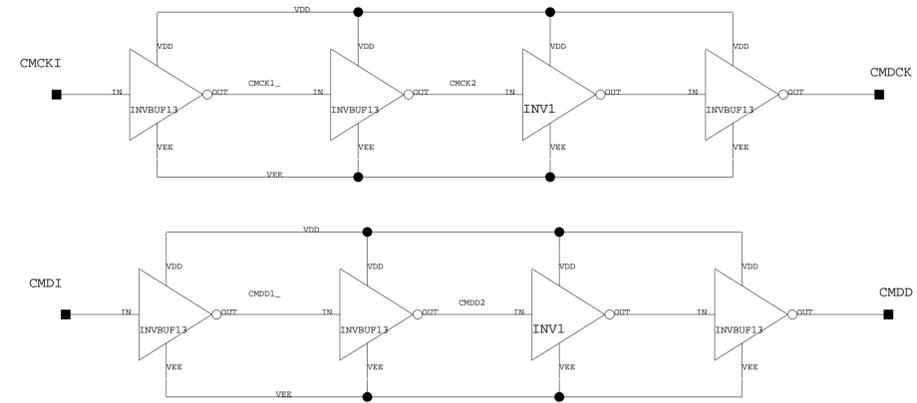
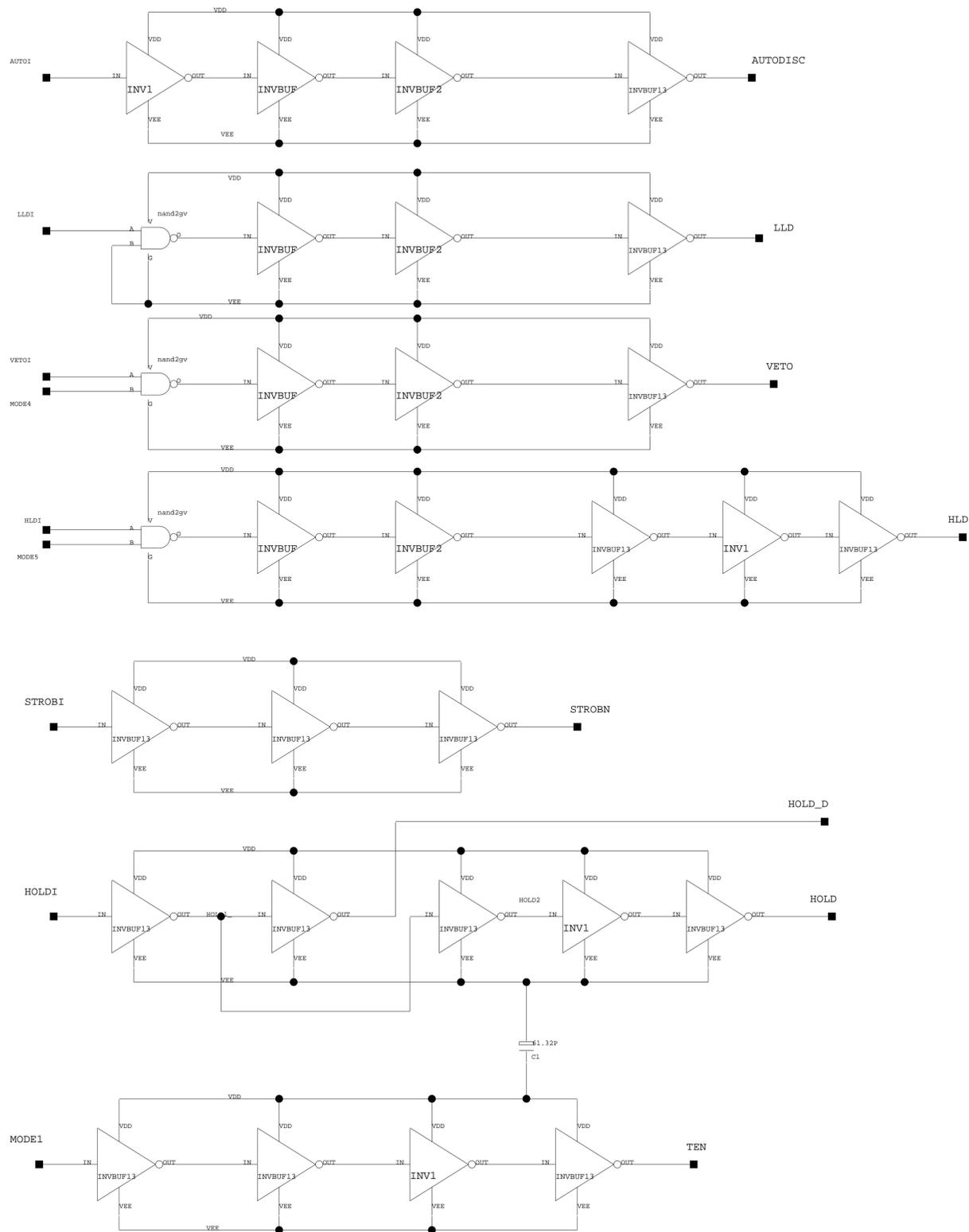
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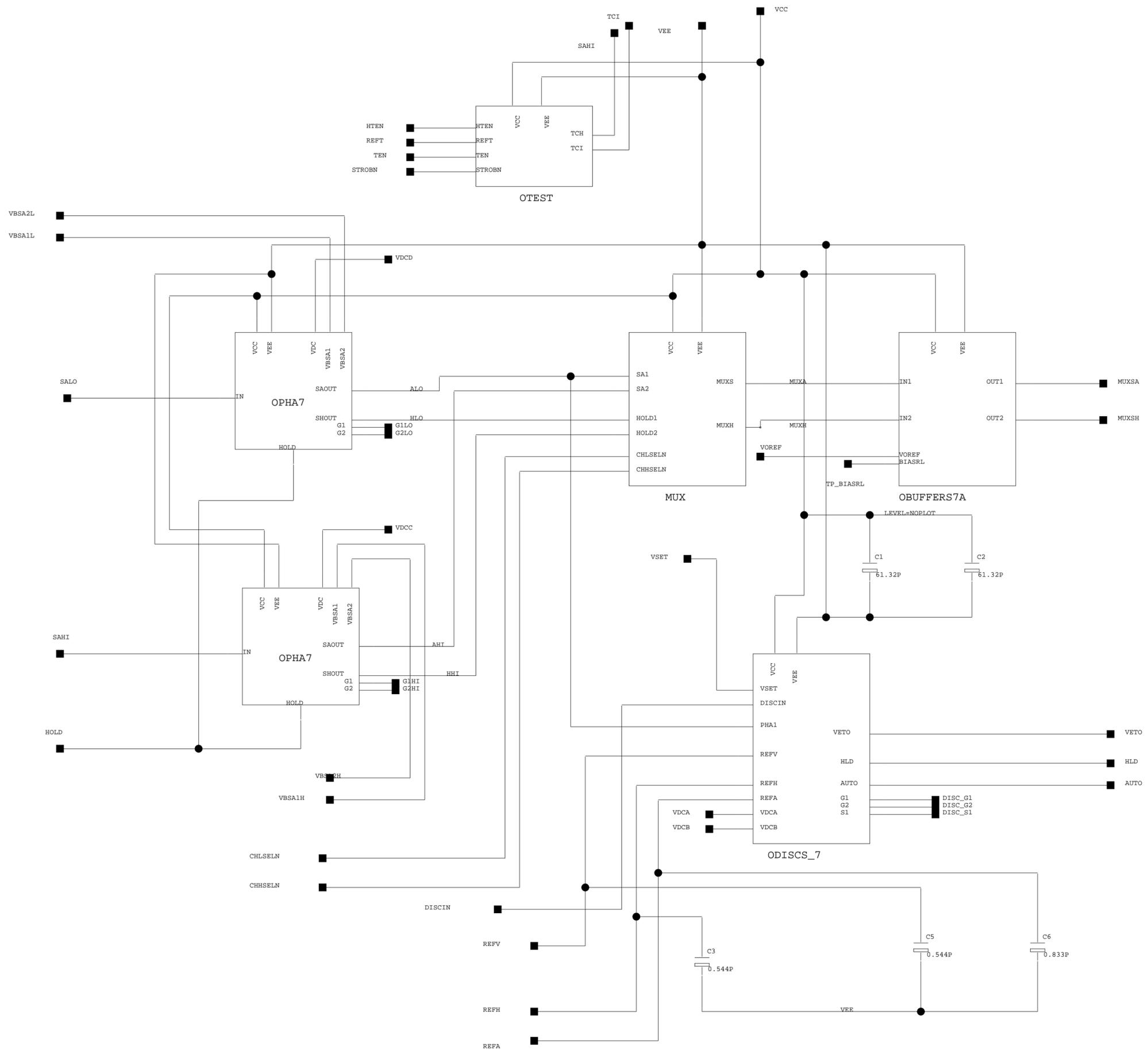
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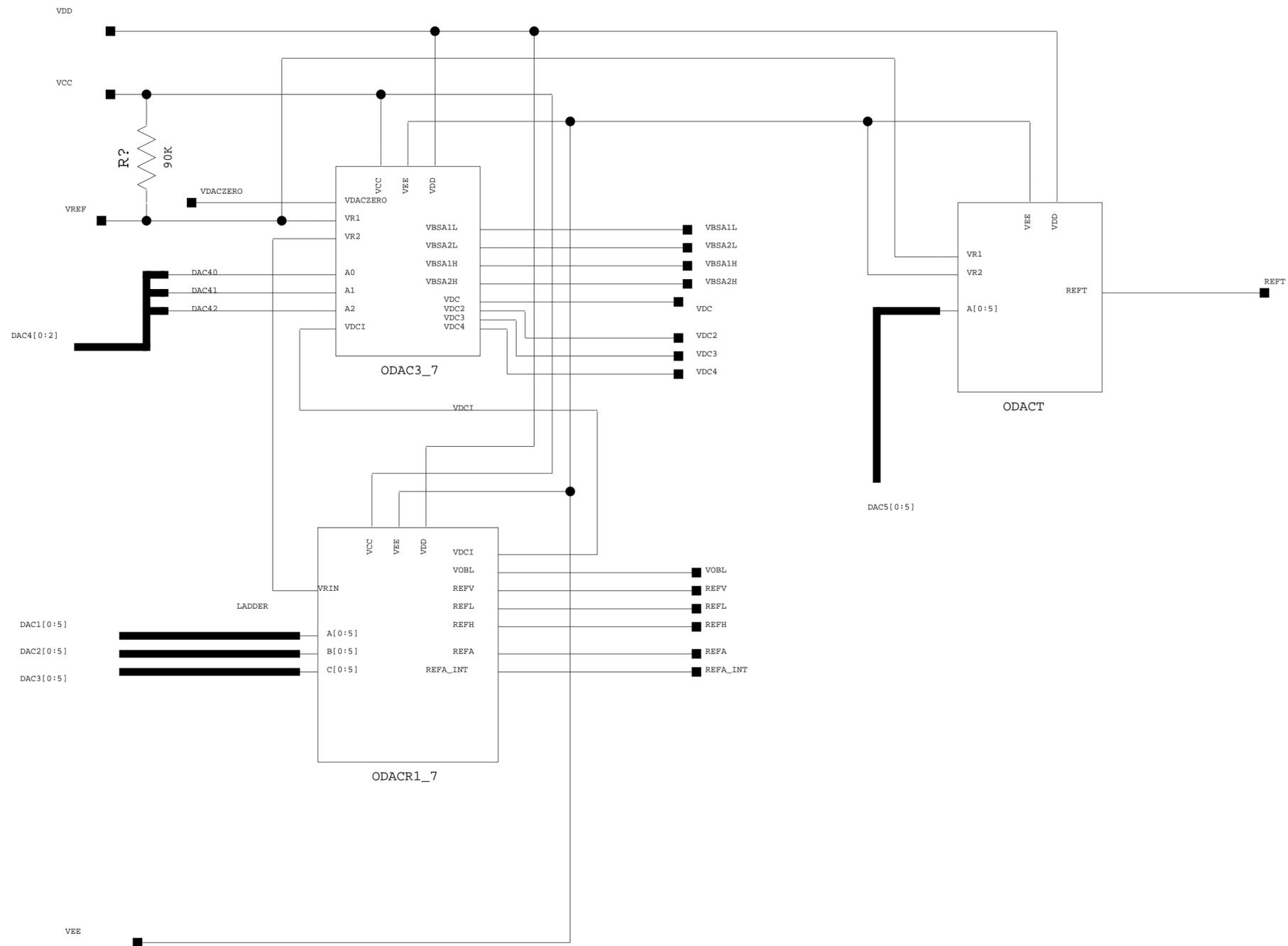
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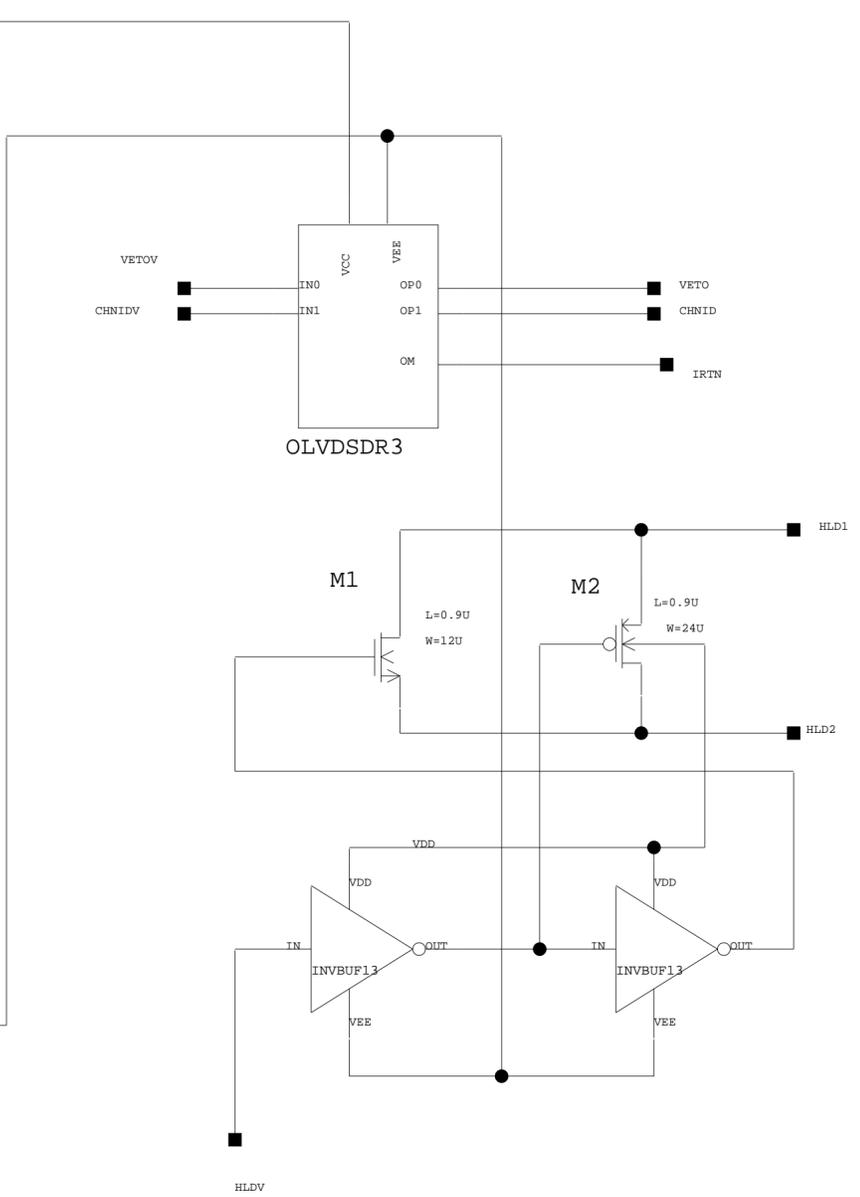
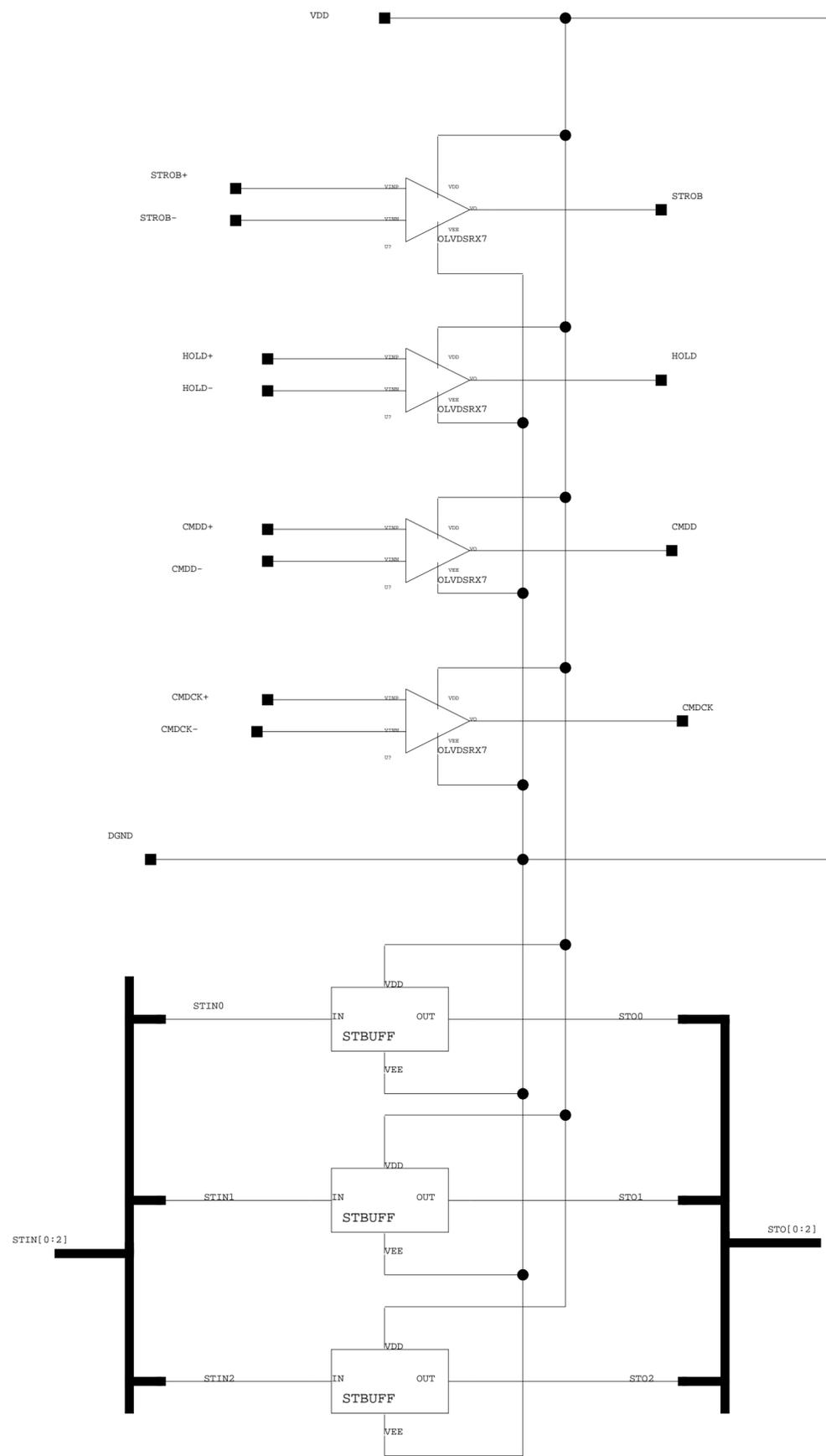
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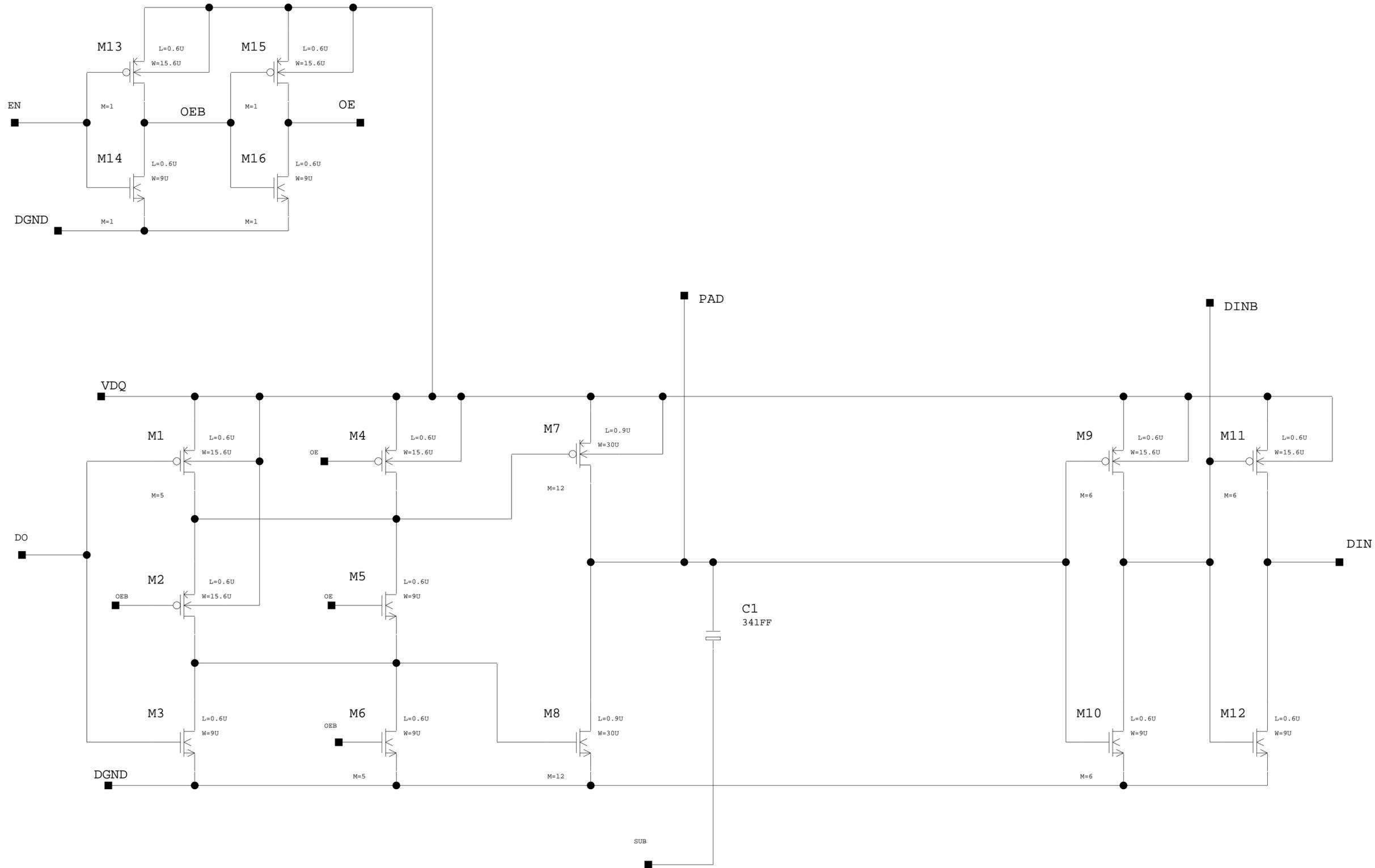
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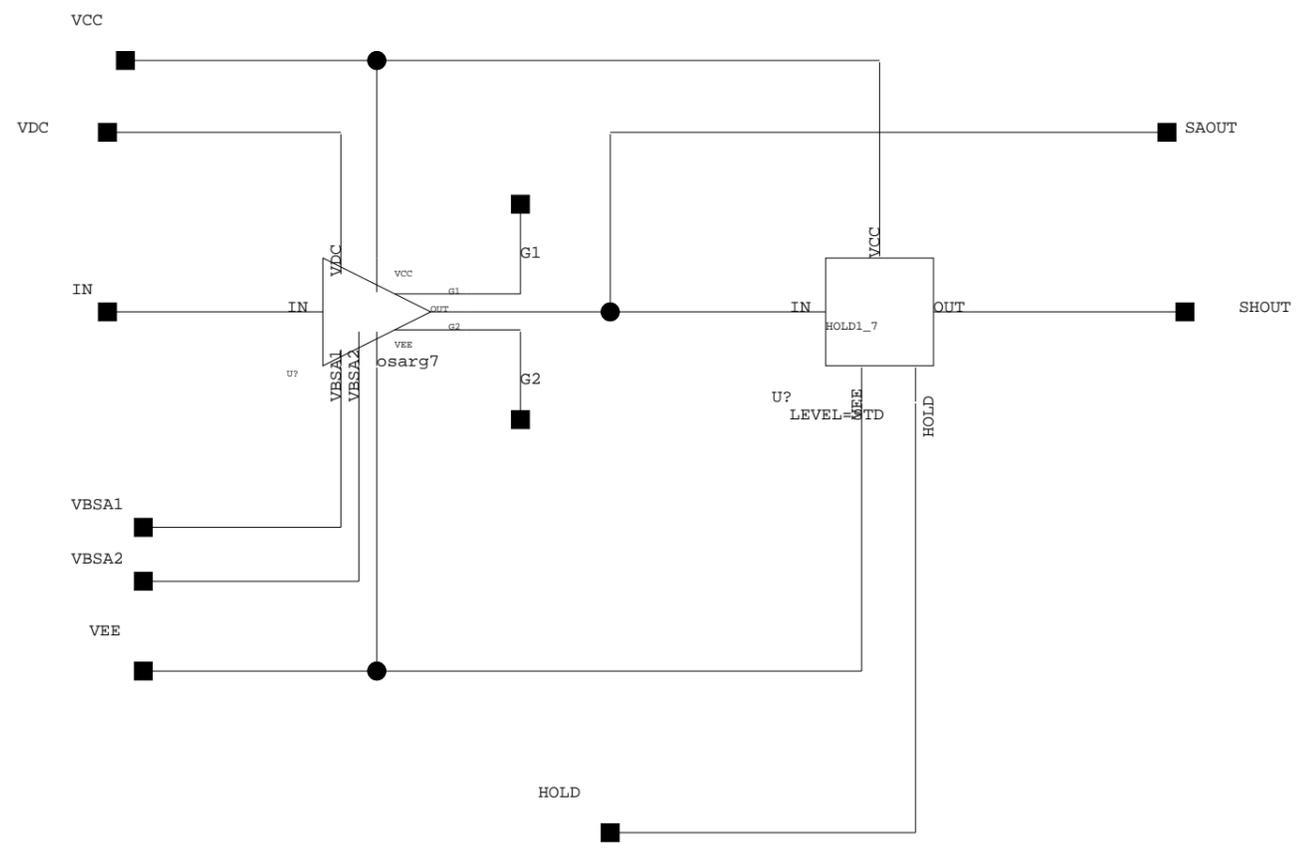
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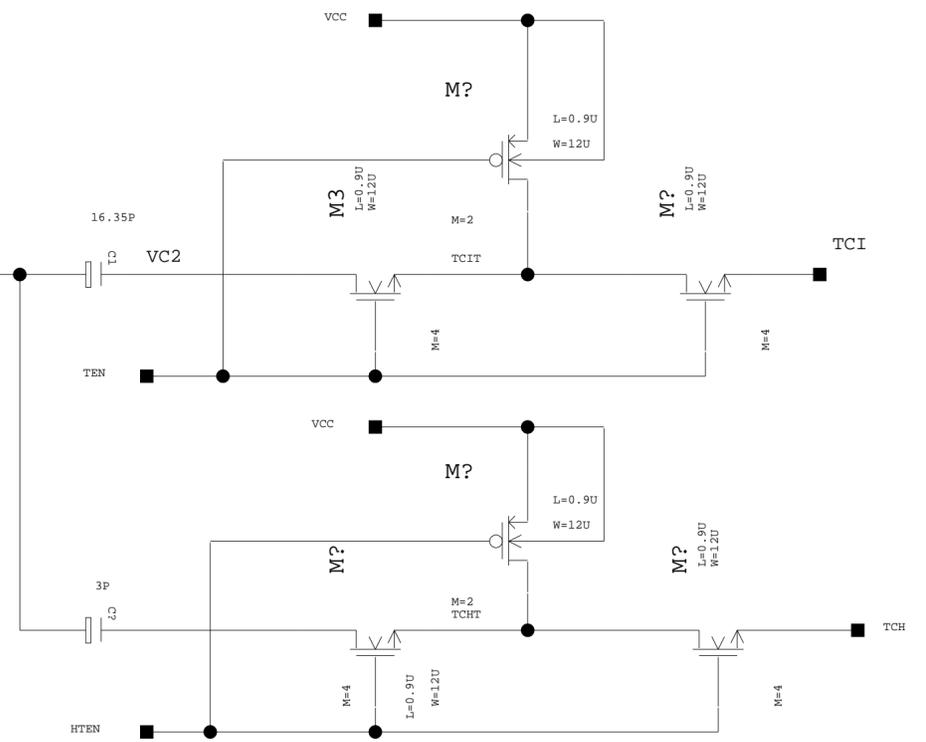
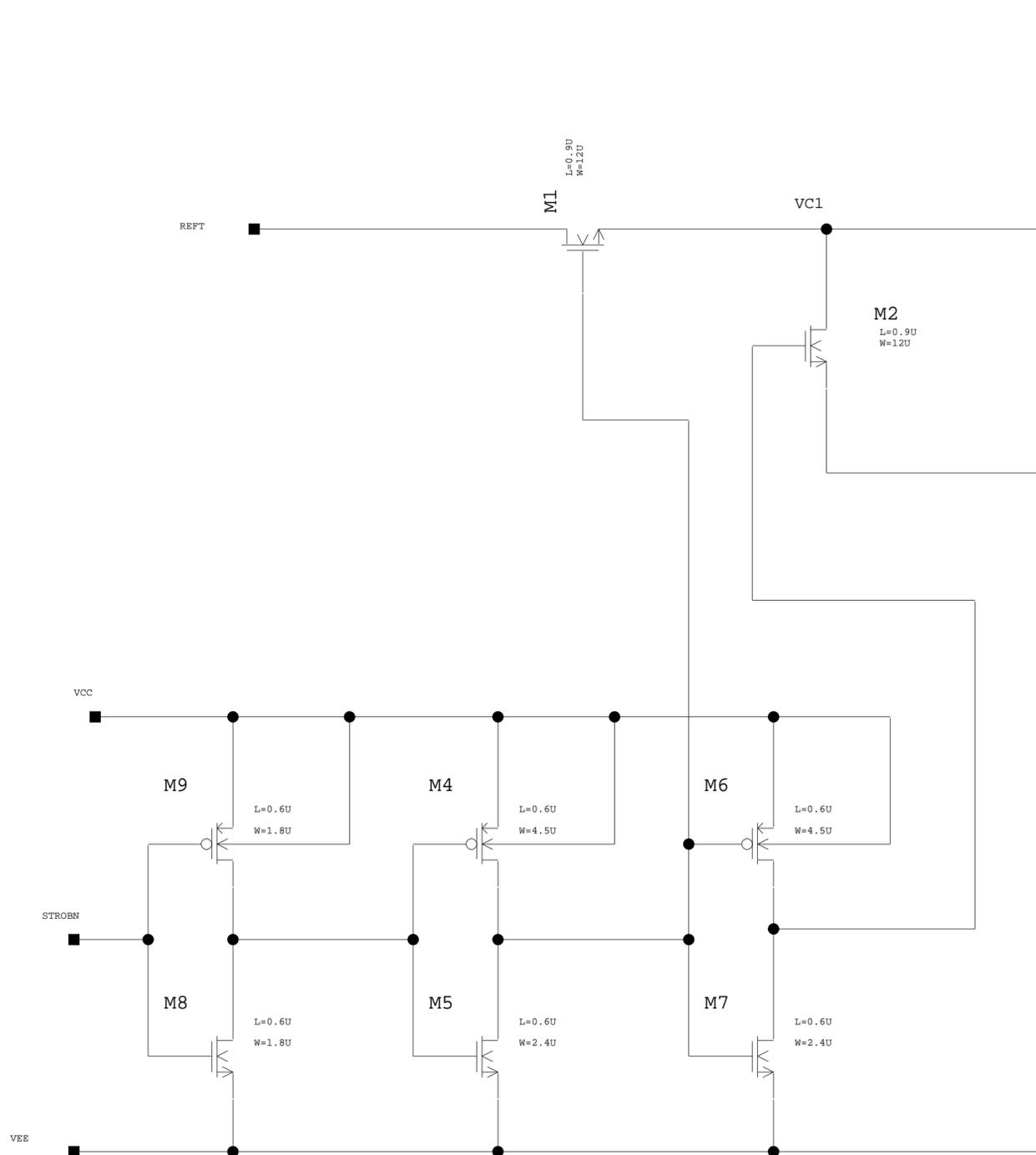
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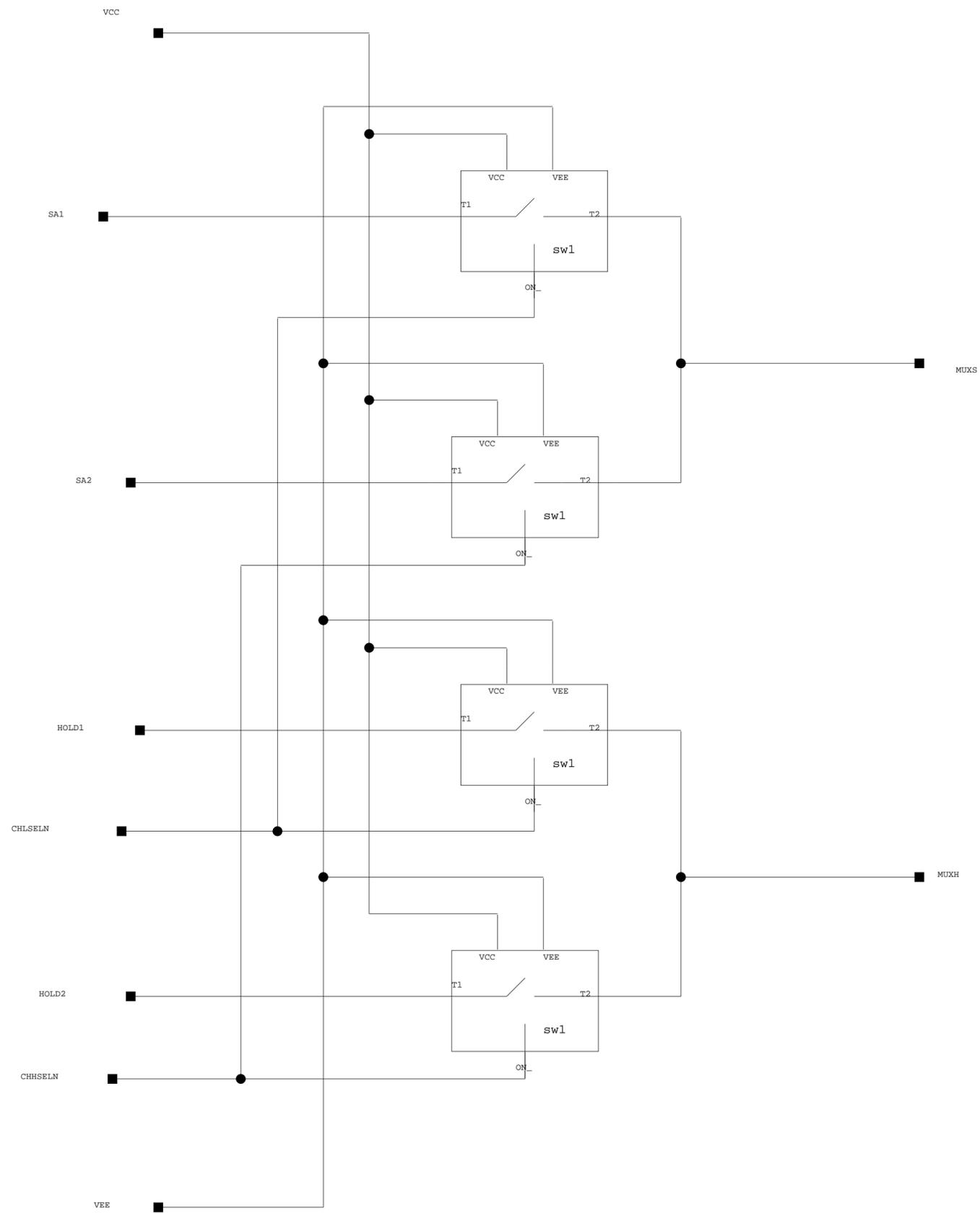
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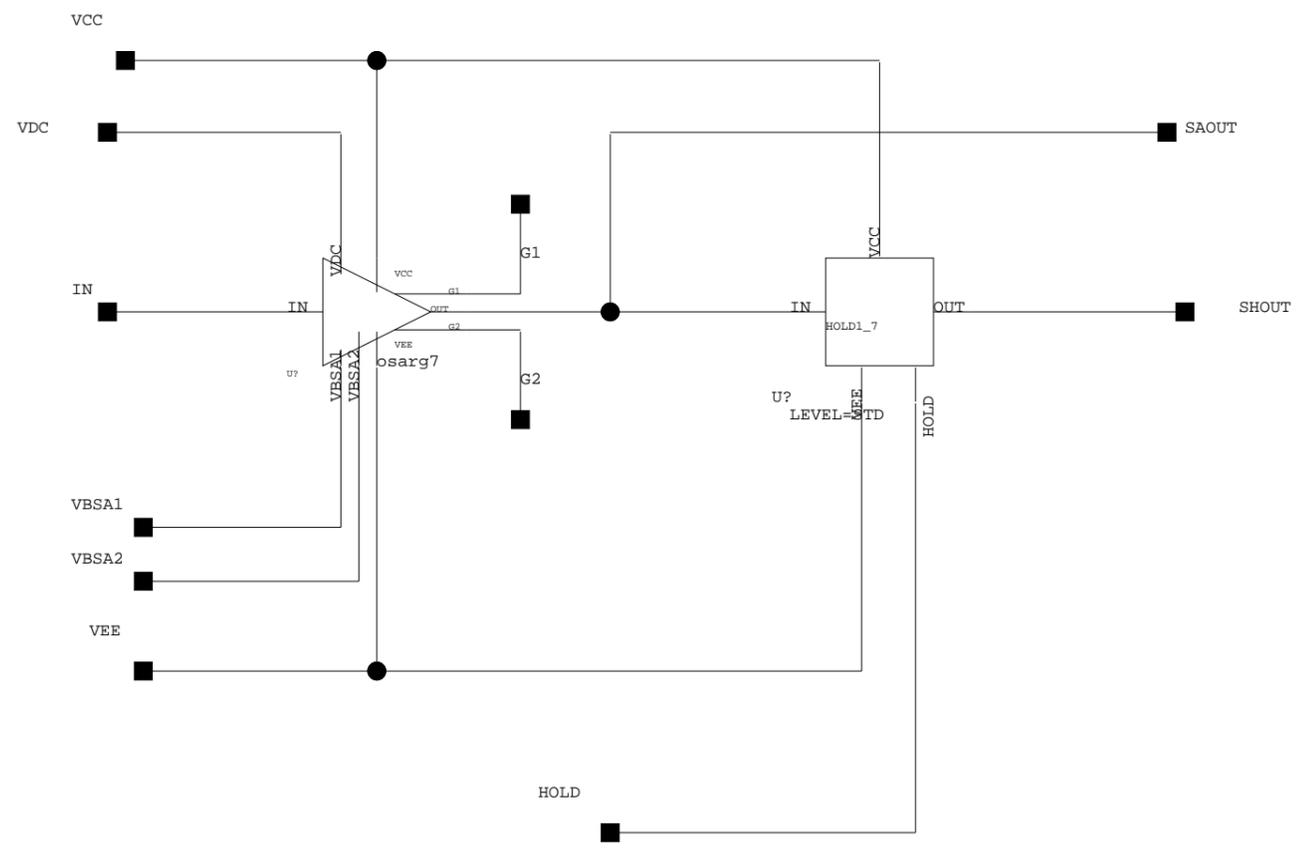
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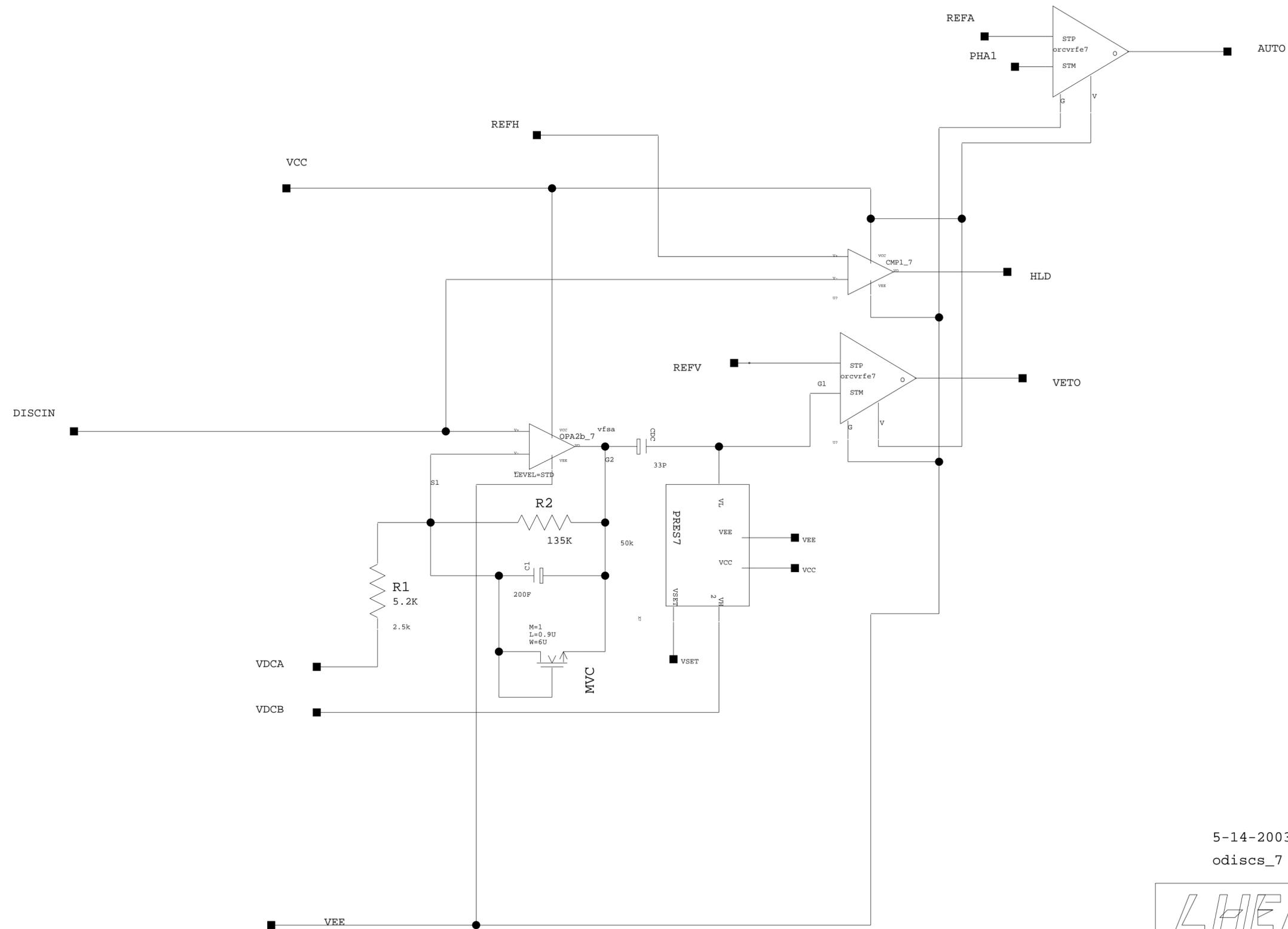
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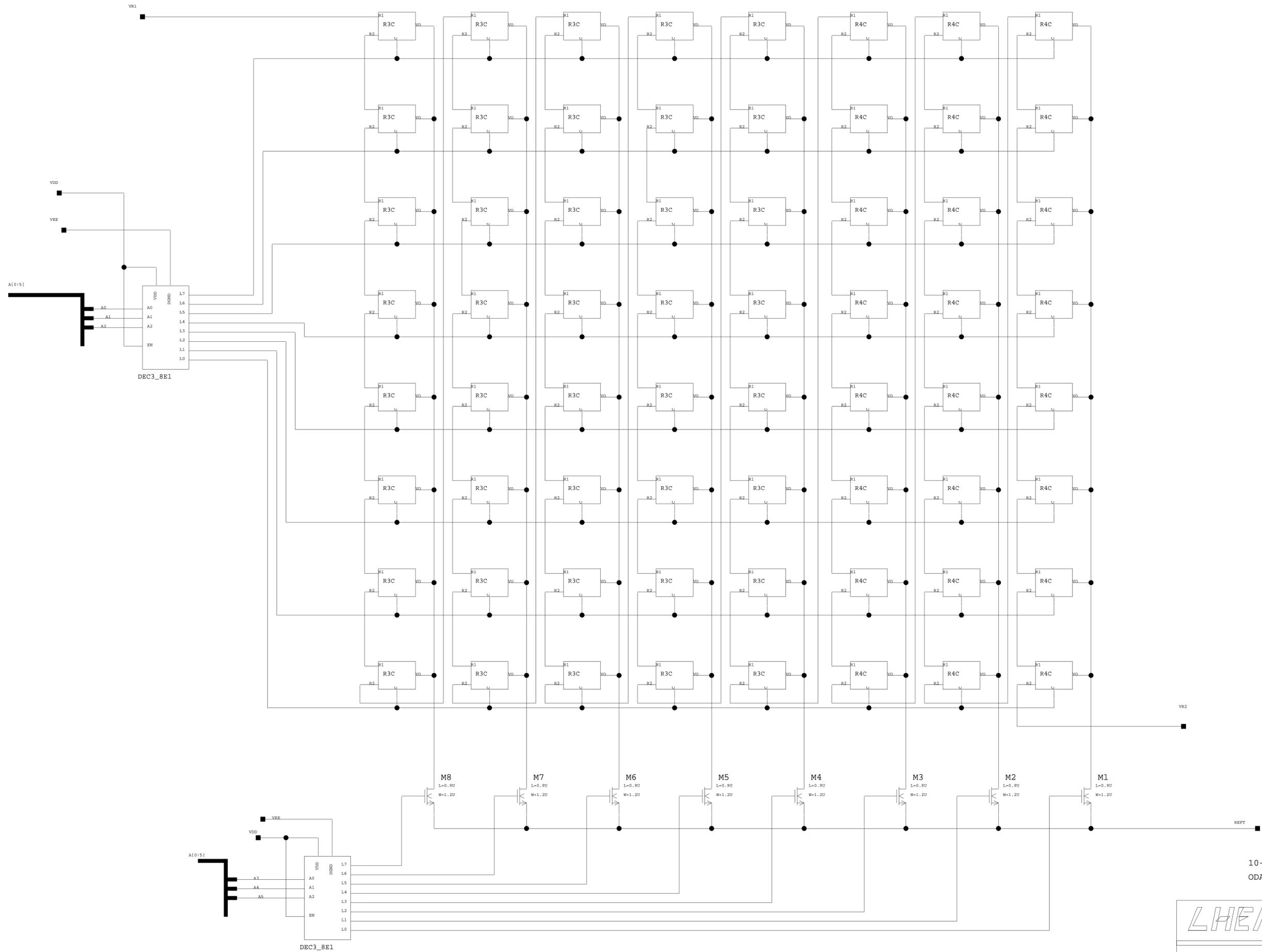
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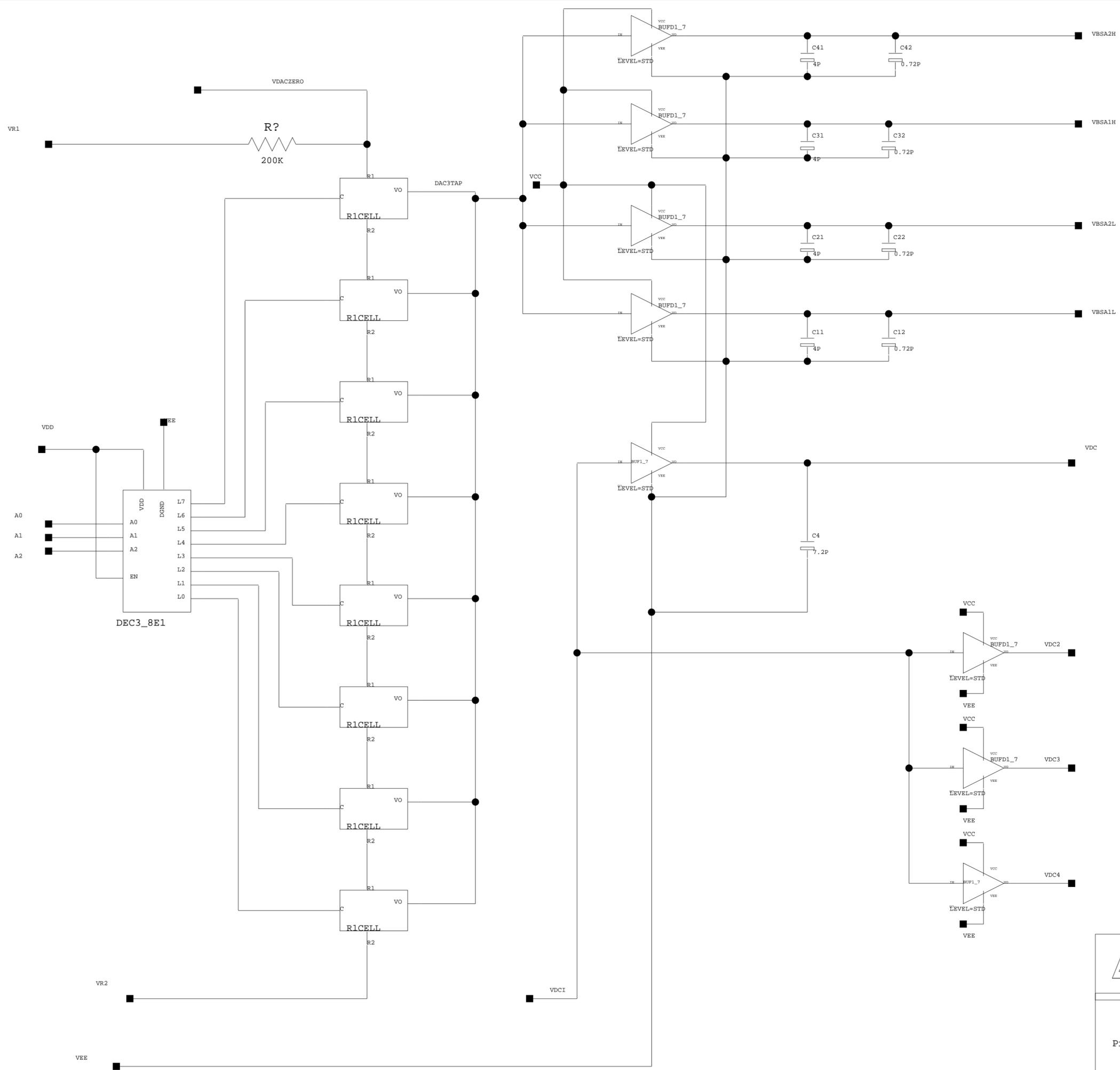
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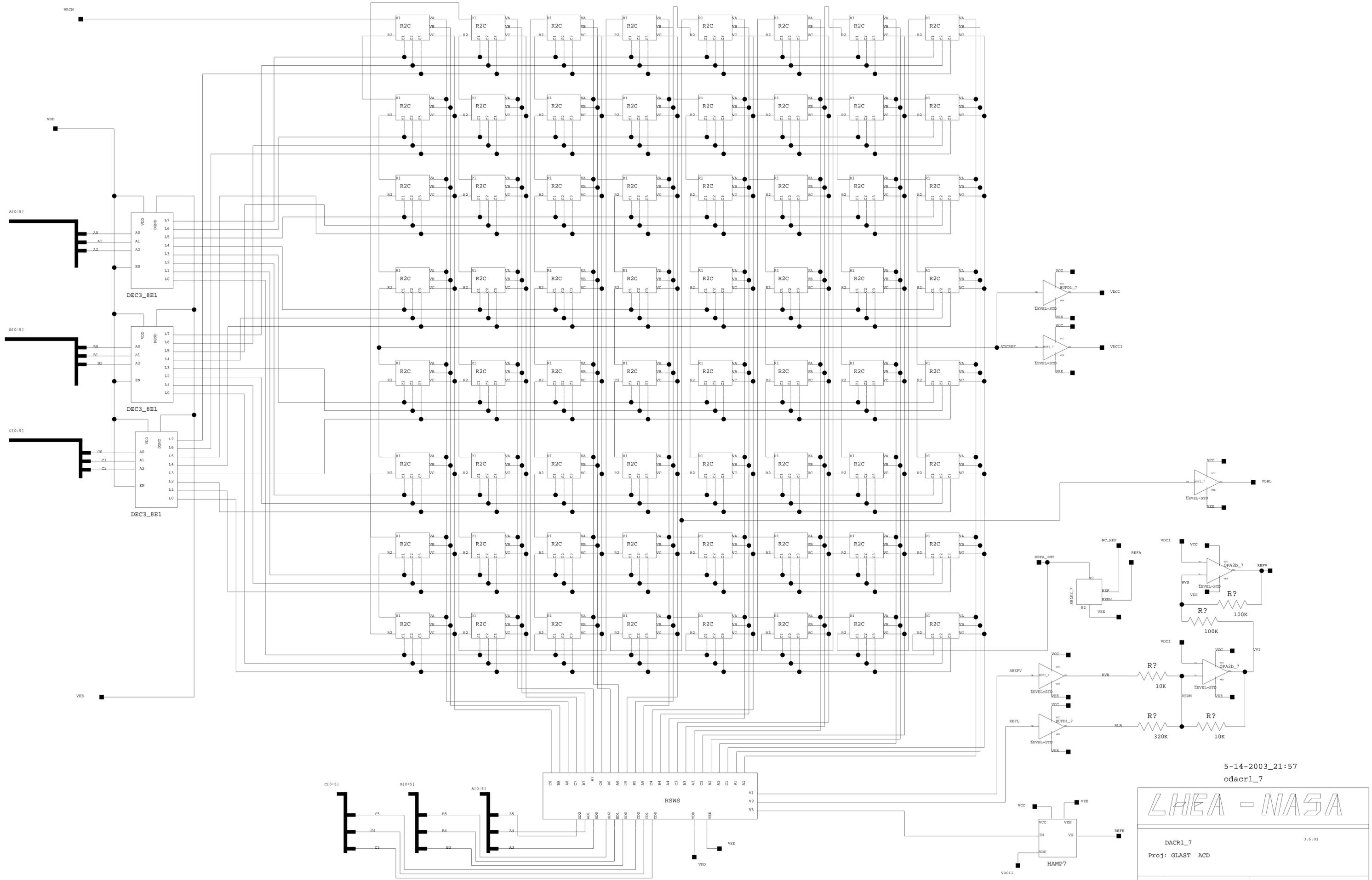
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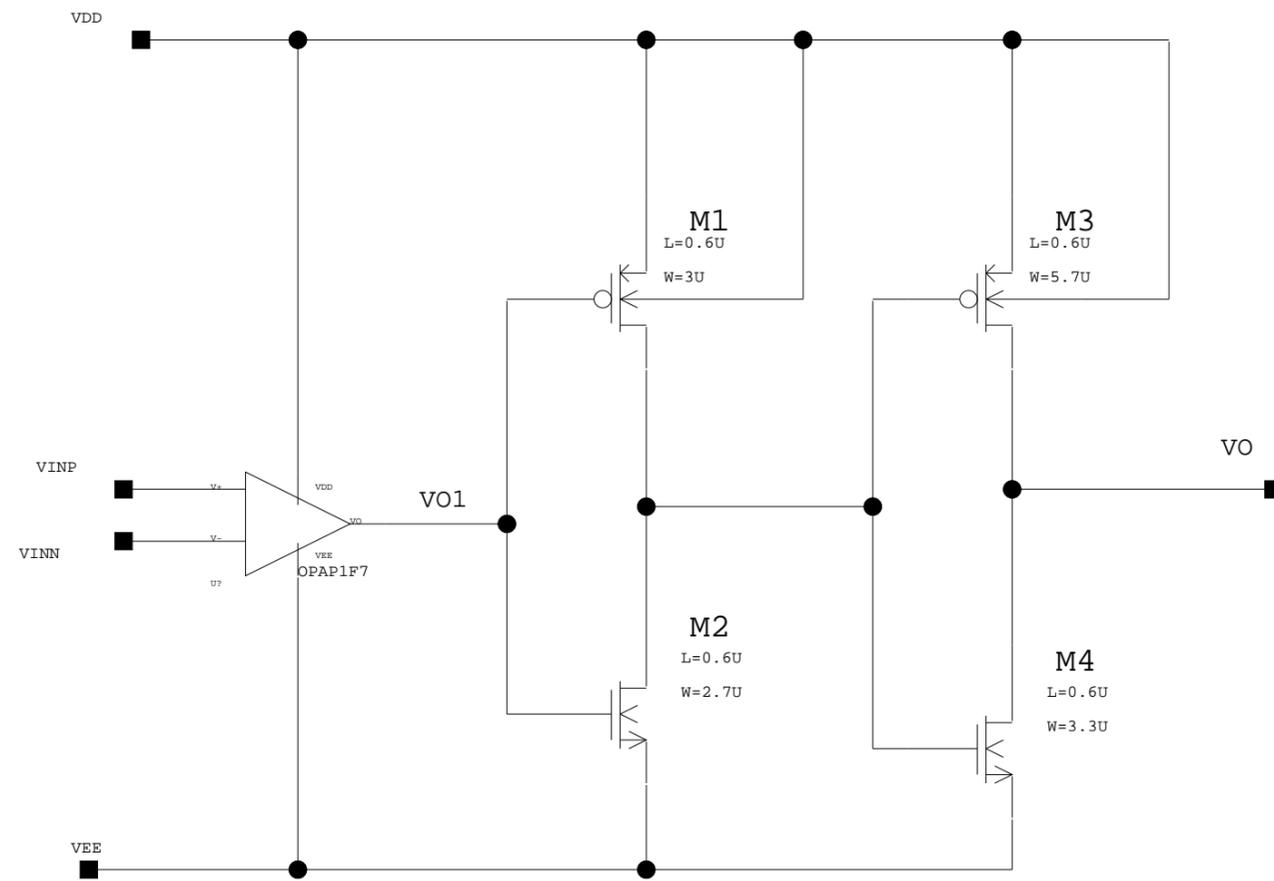
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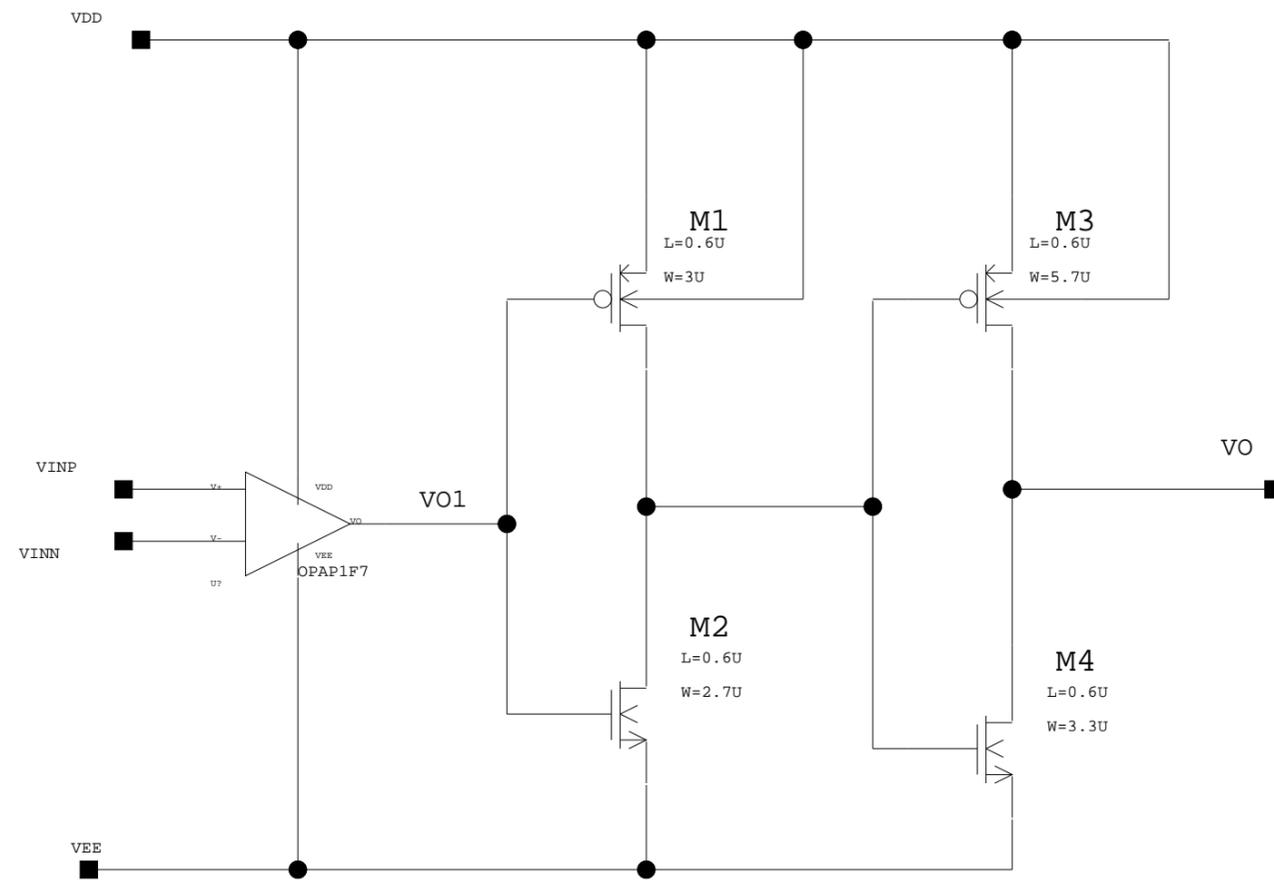
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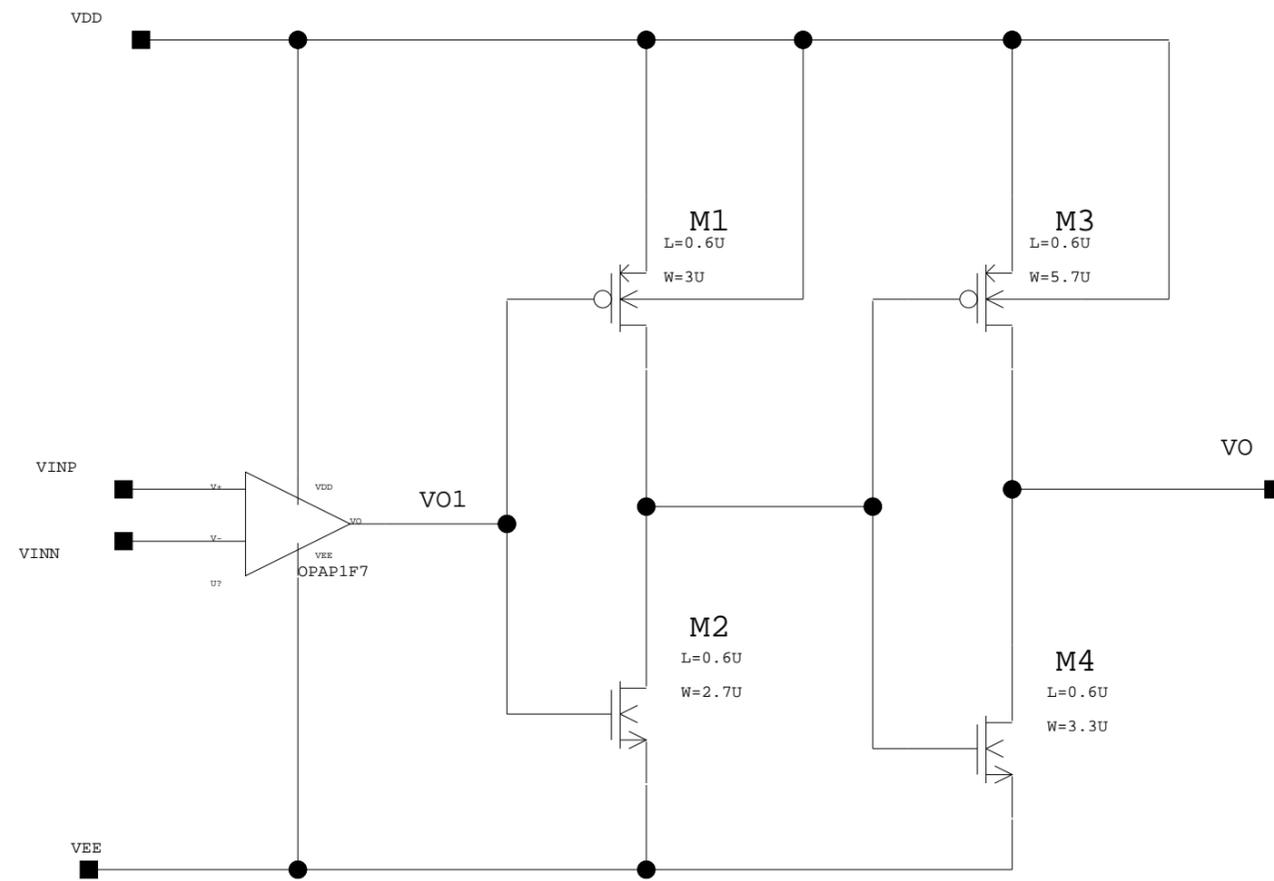
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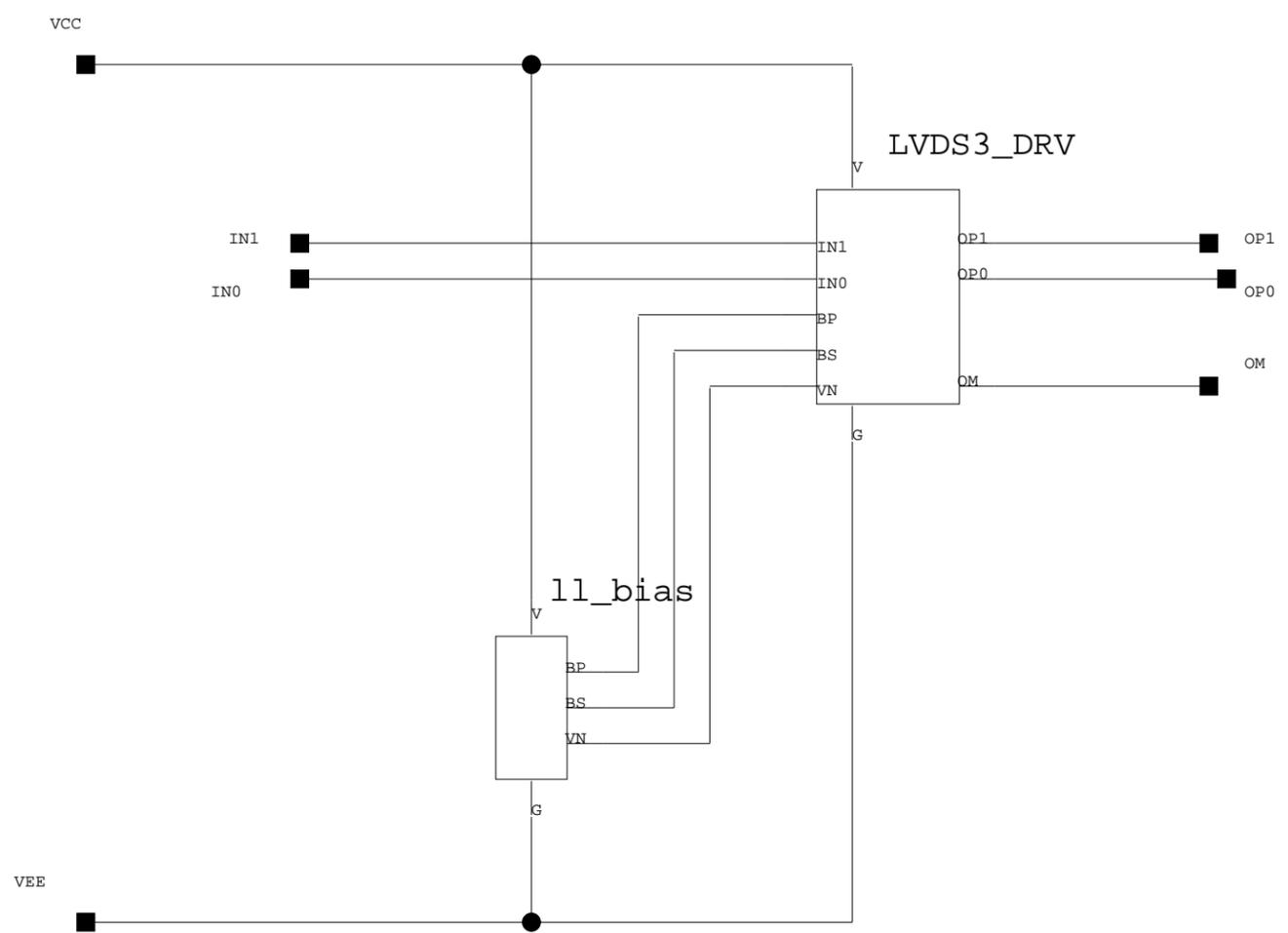
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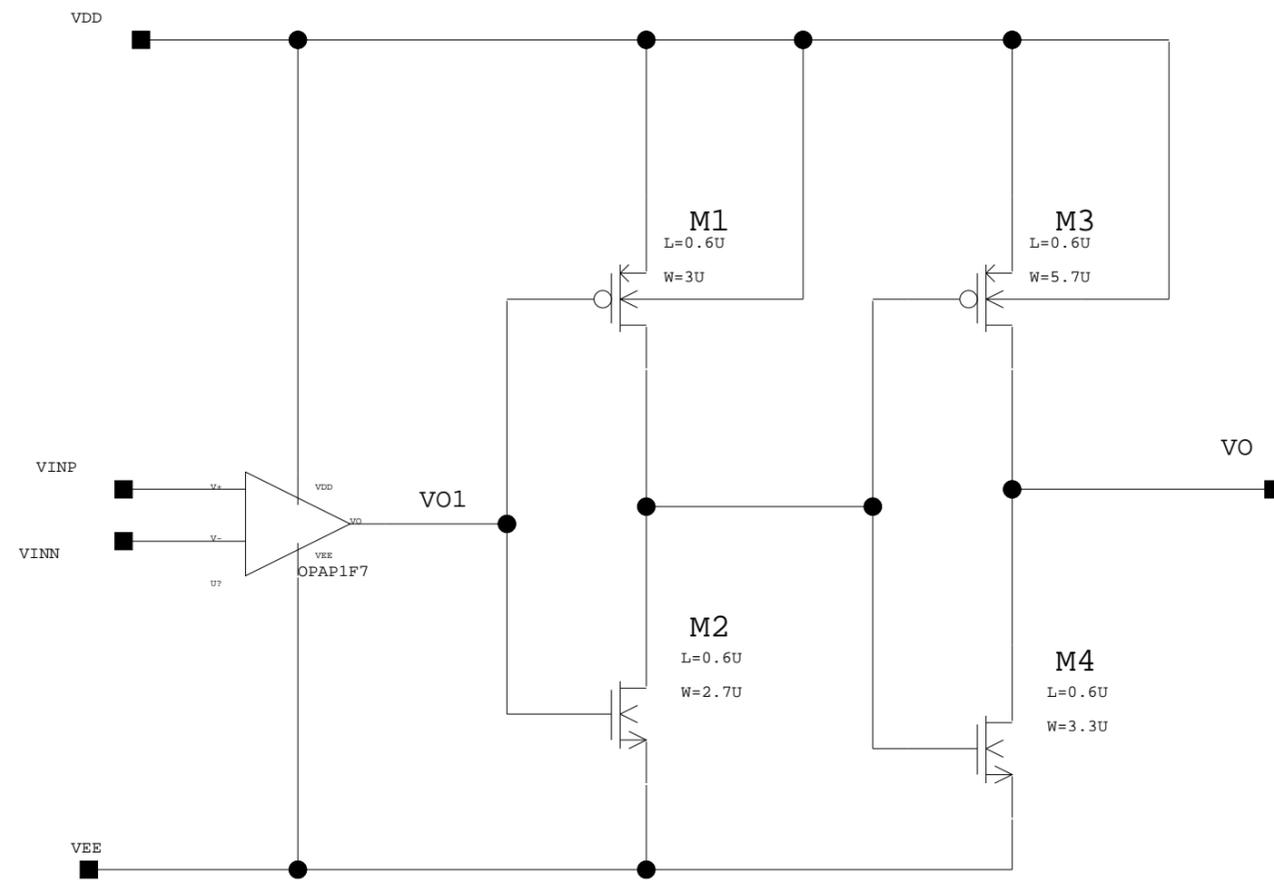
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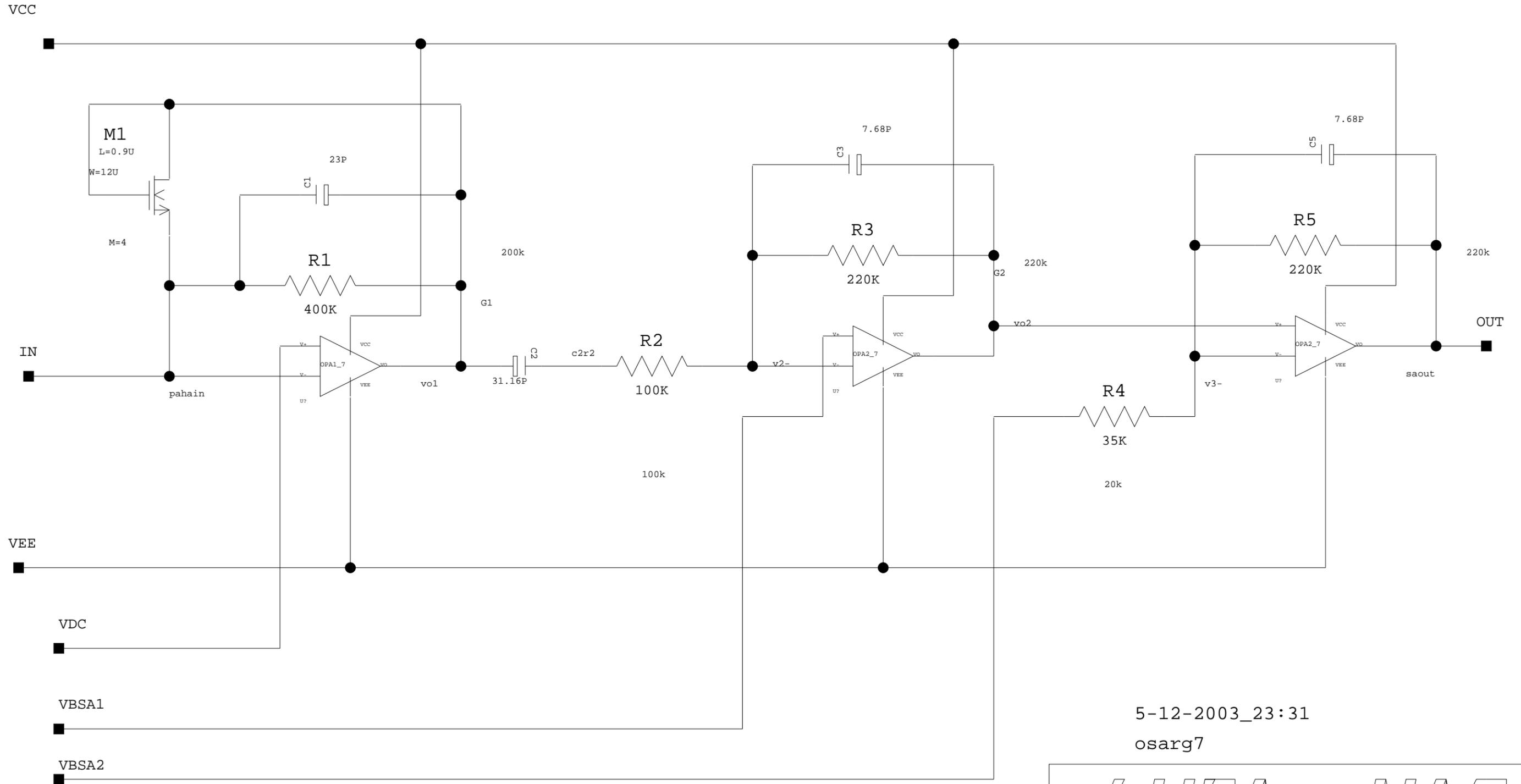
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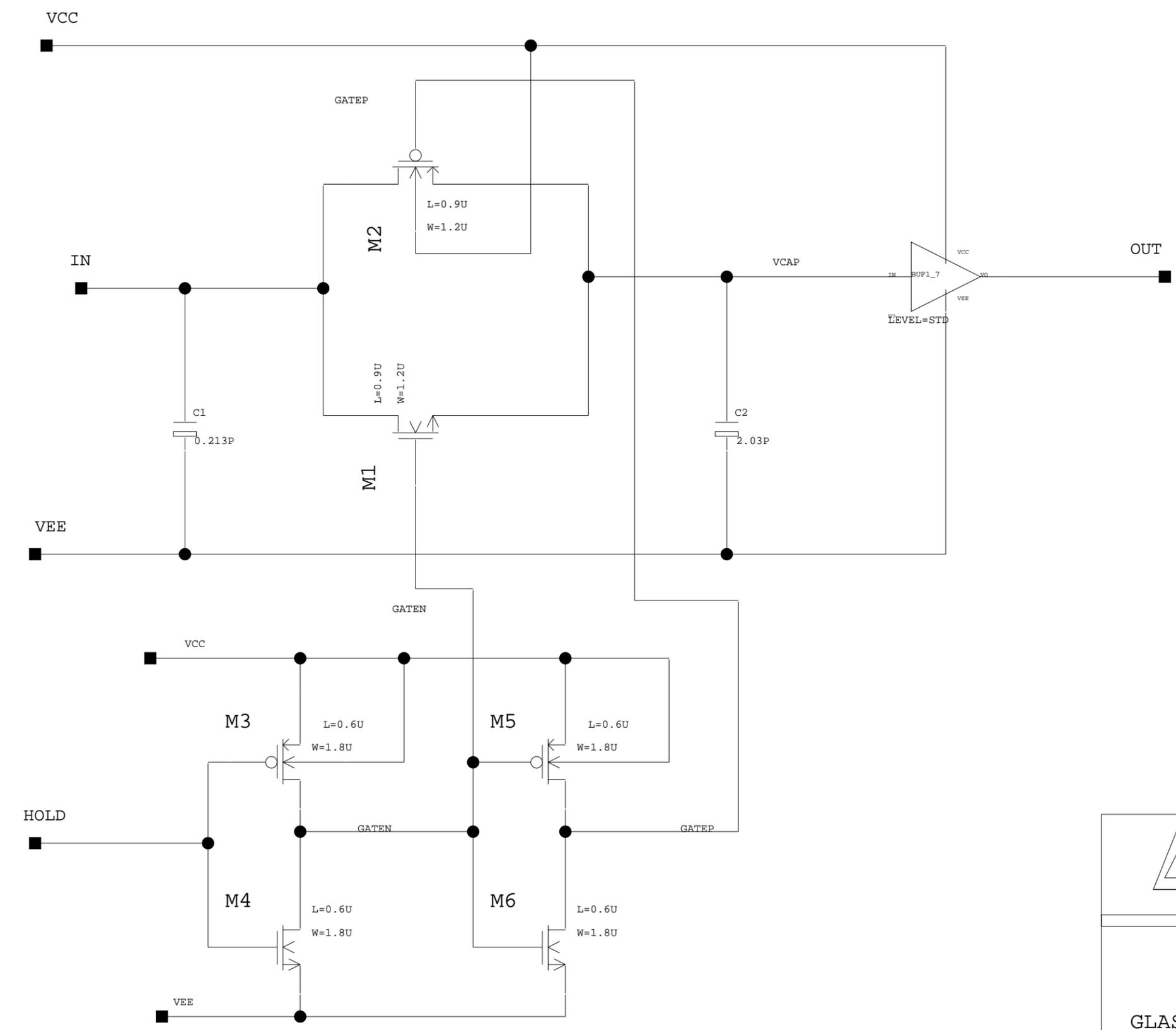
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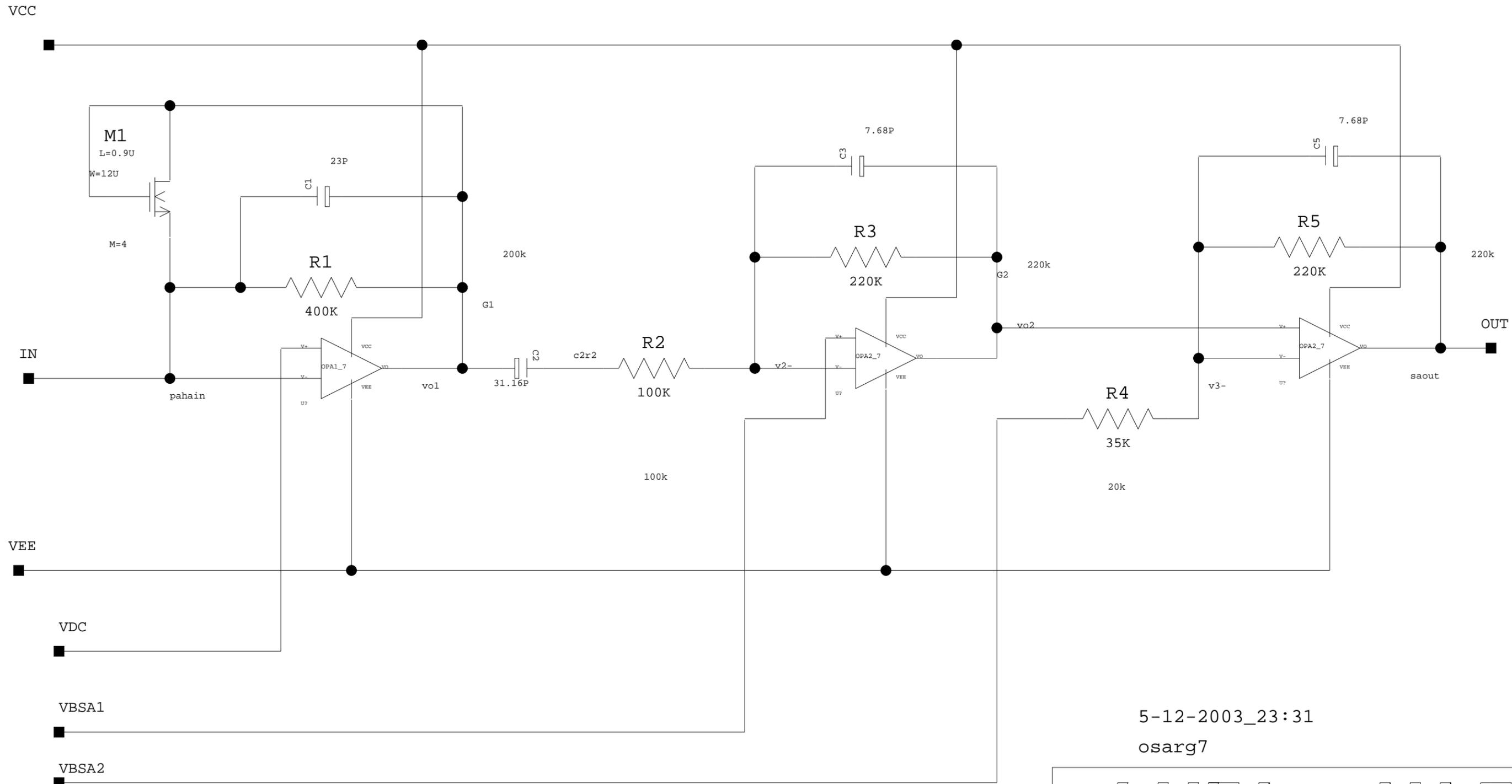
HOLD1_7

GLAST ACD

8.30.01

Ver: GAFE1_1

DRAWN BY: SATPAL SINGH



5-12-2003_23:31
osarg7

LHEA - NASA

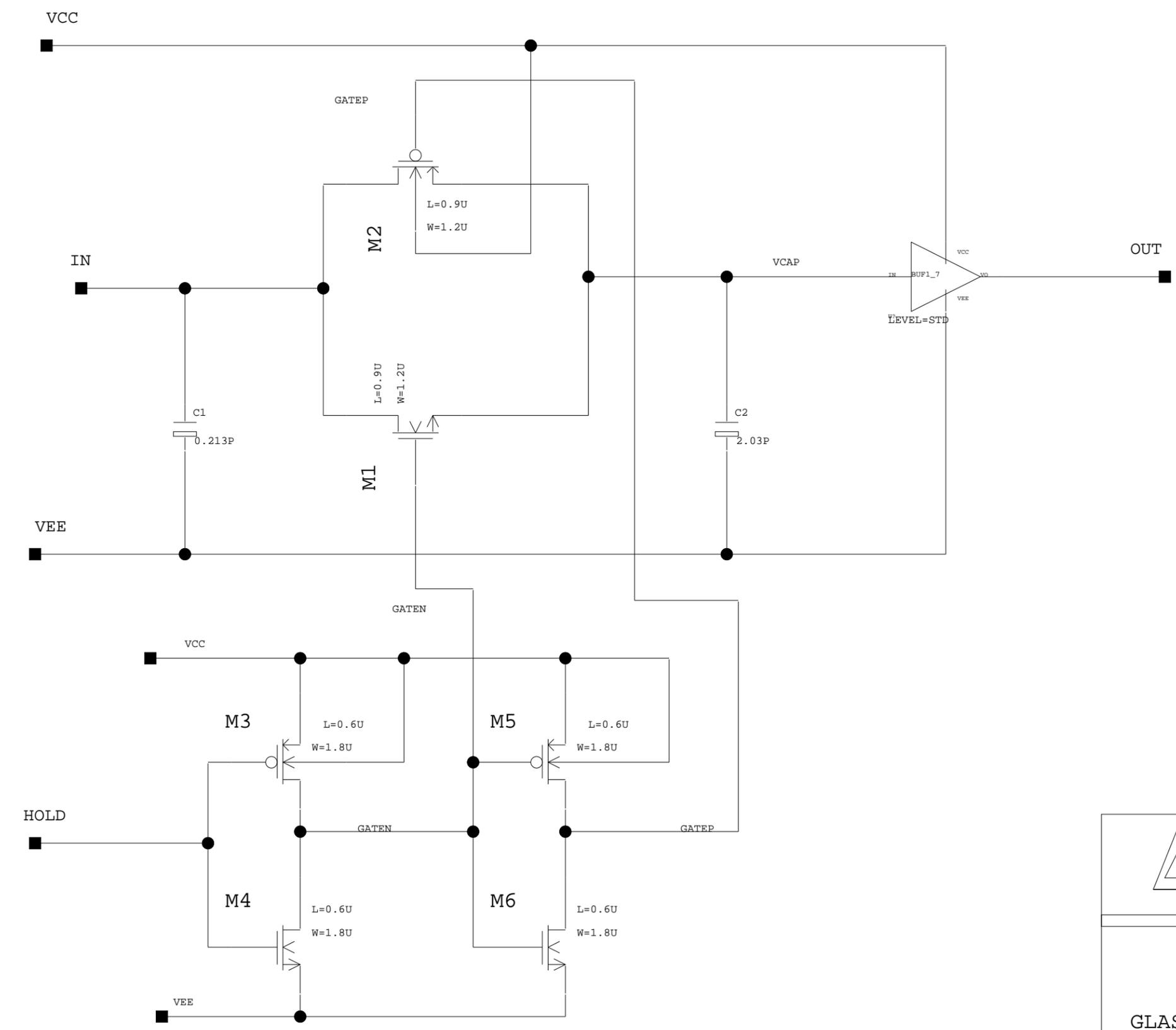
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GLAST ACD

7.18.01

Ver: GAFE1_1

DRAWN BY: OM, SS



4-24-2003_23:16
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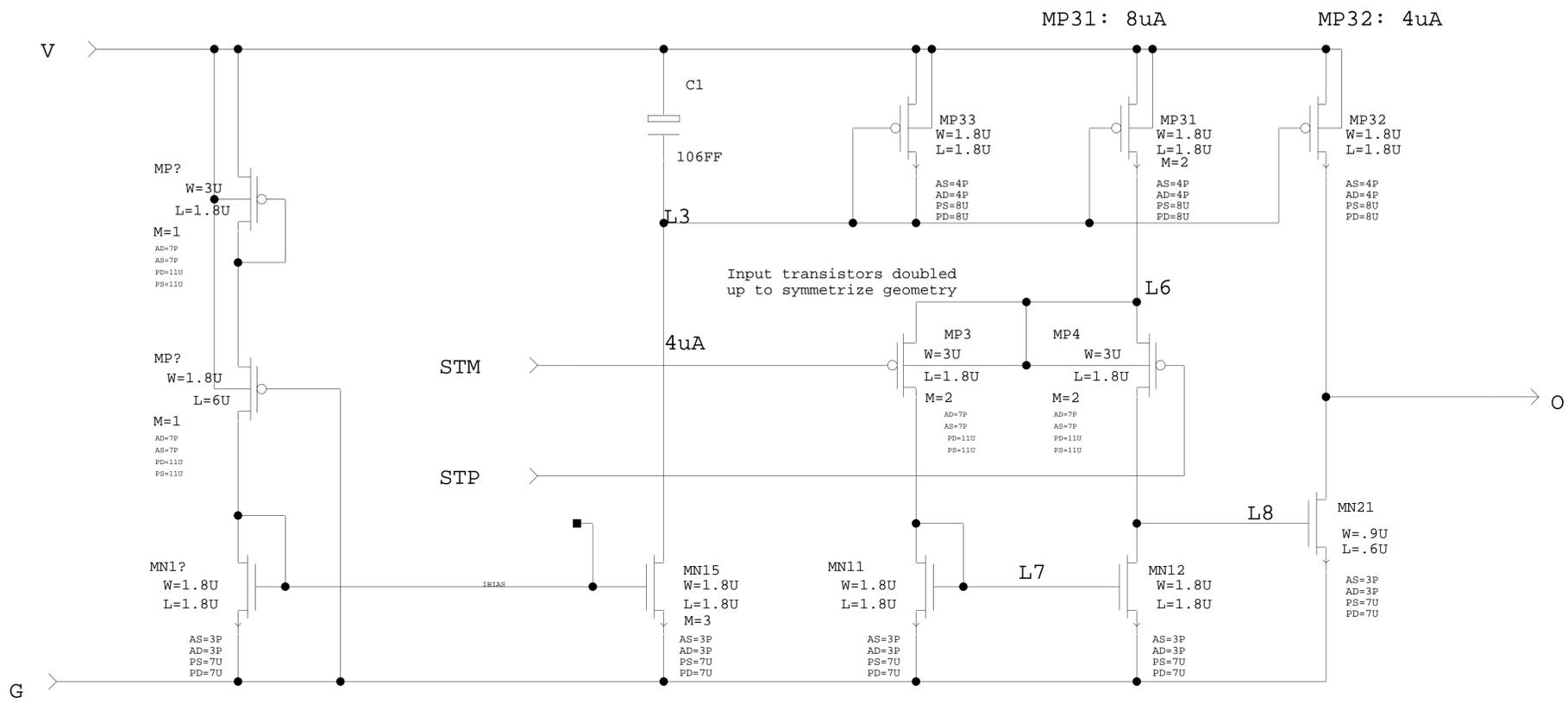
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GLAST ACD

8.30.01

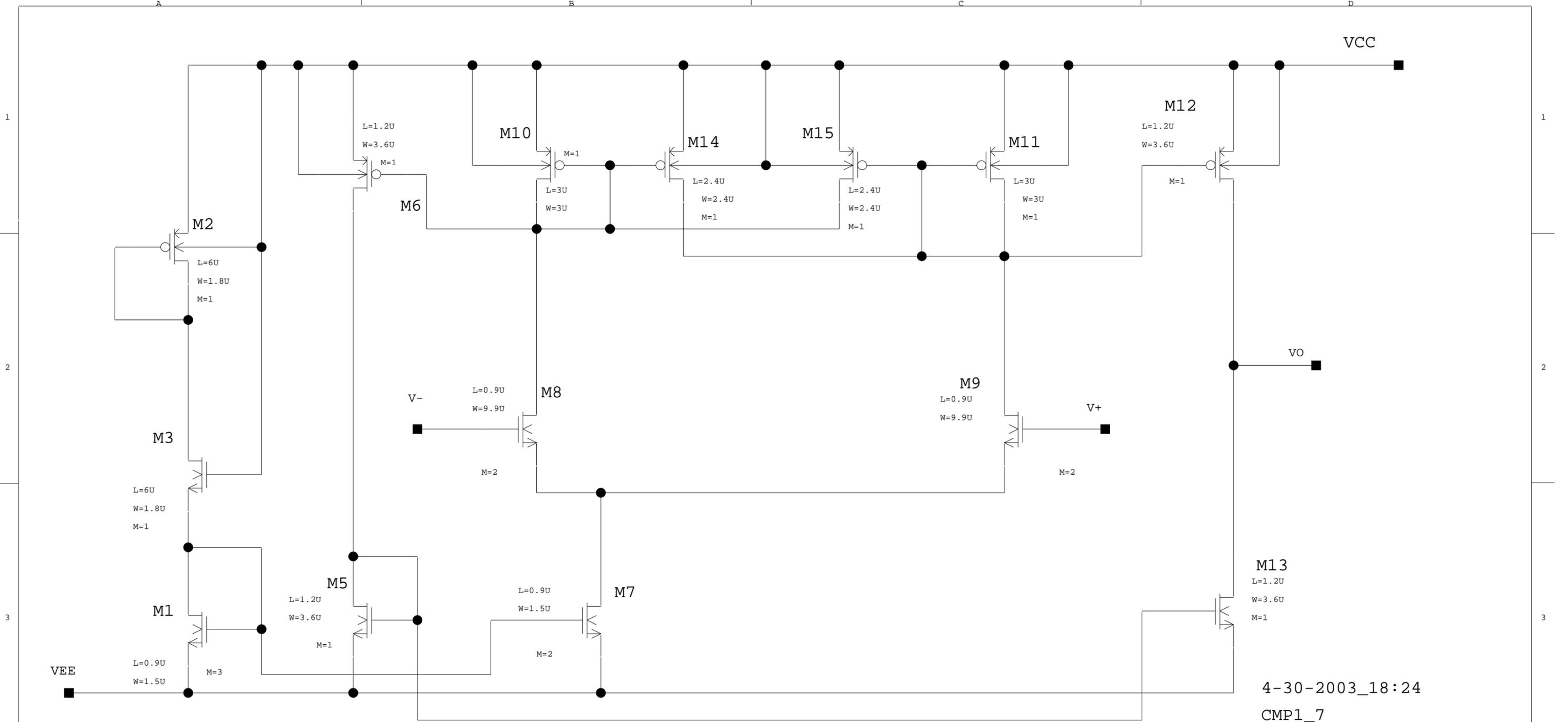
Ver: GAFE1_1

DRAWN BY: SATPAL SINGH



gcfe4: MN15 M=4, MP31 M=4 -> I=14u
gcfe2: MN15 M=3, MP31 M=2 -> I=6u
gcfe3: same as gcfe2

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ENGR	DATE	APPROVALS



VIEWlogic™

CMP1_7

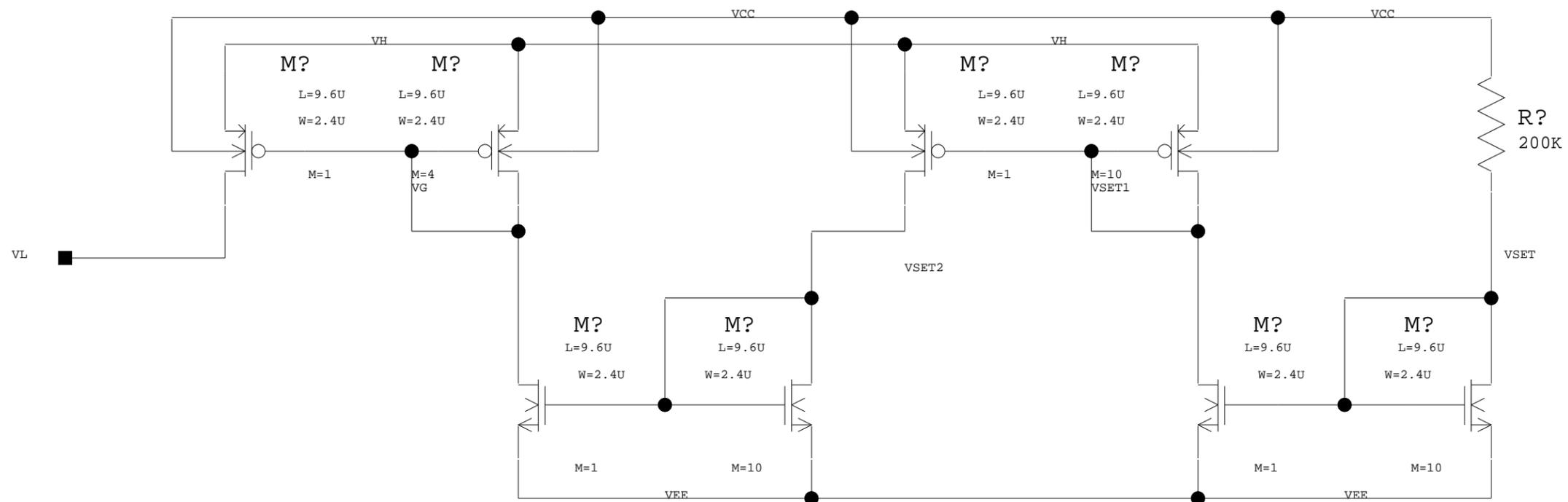
GLAST / ACD. -Per0.5u

12.13.00

Ver: GAFE1_1

DRAWN BY:

SATPAL SINGH

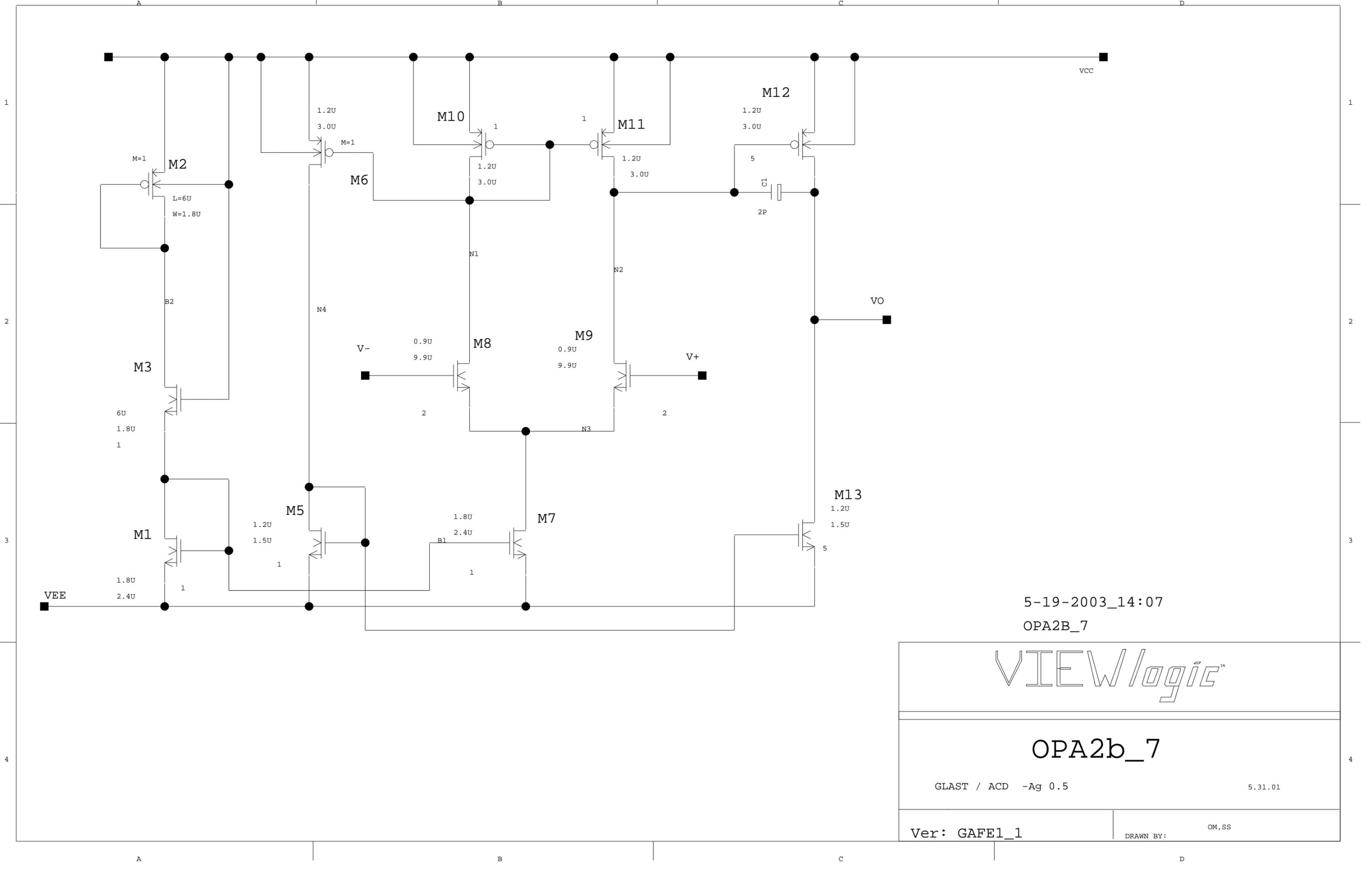


Stanford Linear Accelerator Cent

PRES
adjustable mosfet resistor

OM 22OCT08

DRAWN BY: Oren Milgrome



5-19-2003_14:07
 OPA2B_7

VIEWlogic™

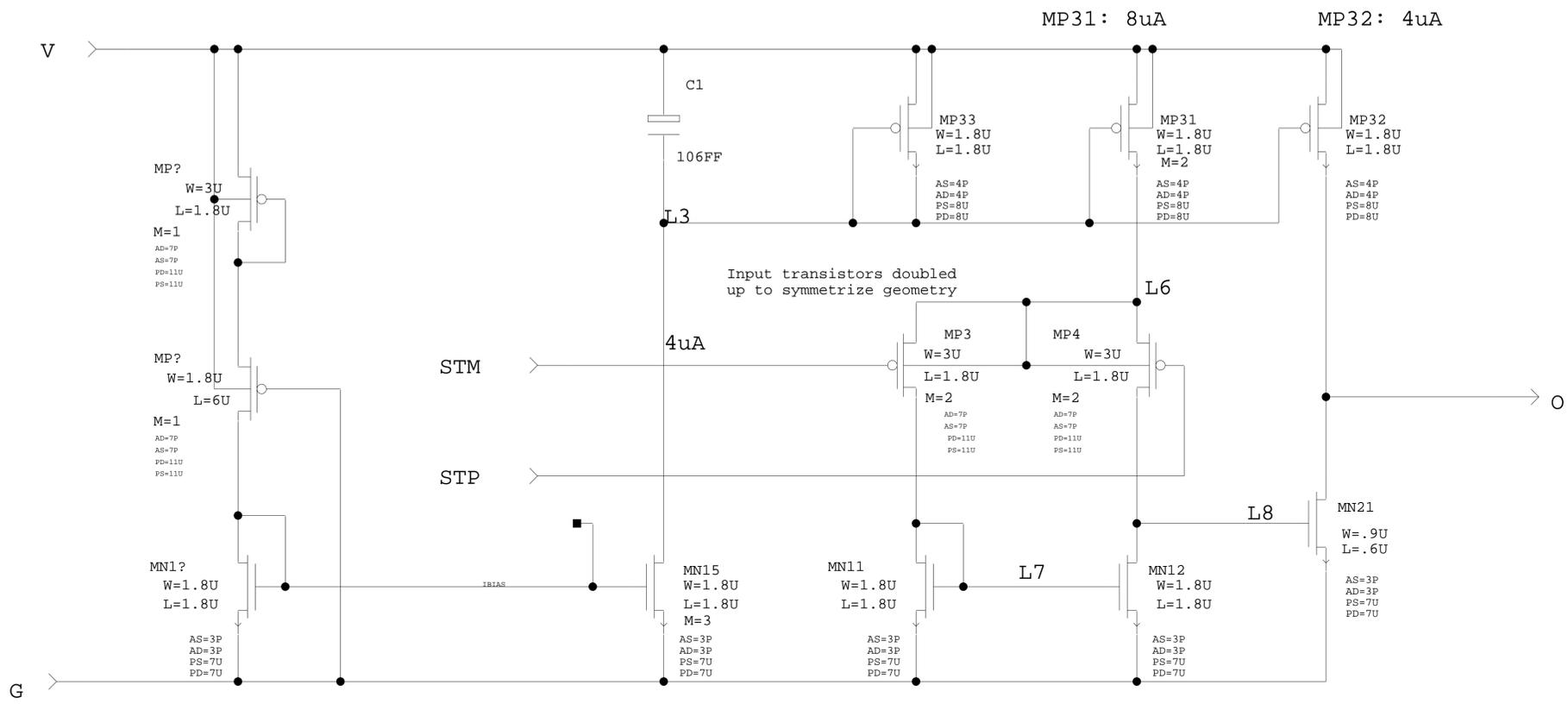
OPA2b_7

GLAST / ACD -Ag 0.5

5.31.01

Ver: GAFE1_1

DRAWN BY: OM,SS

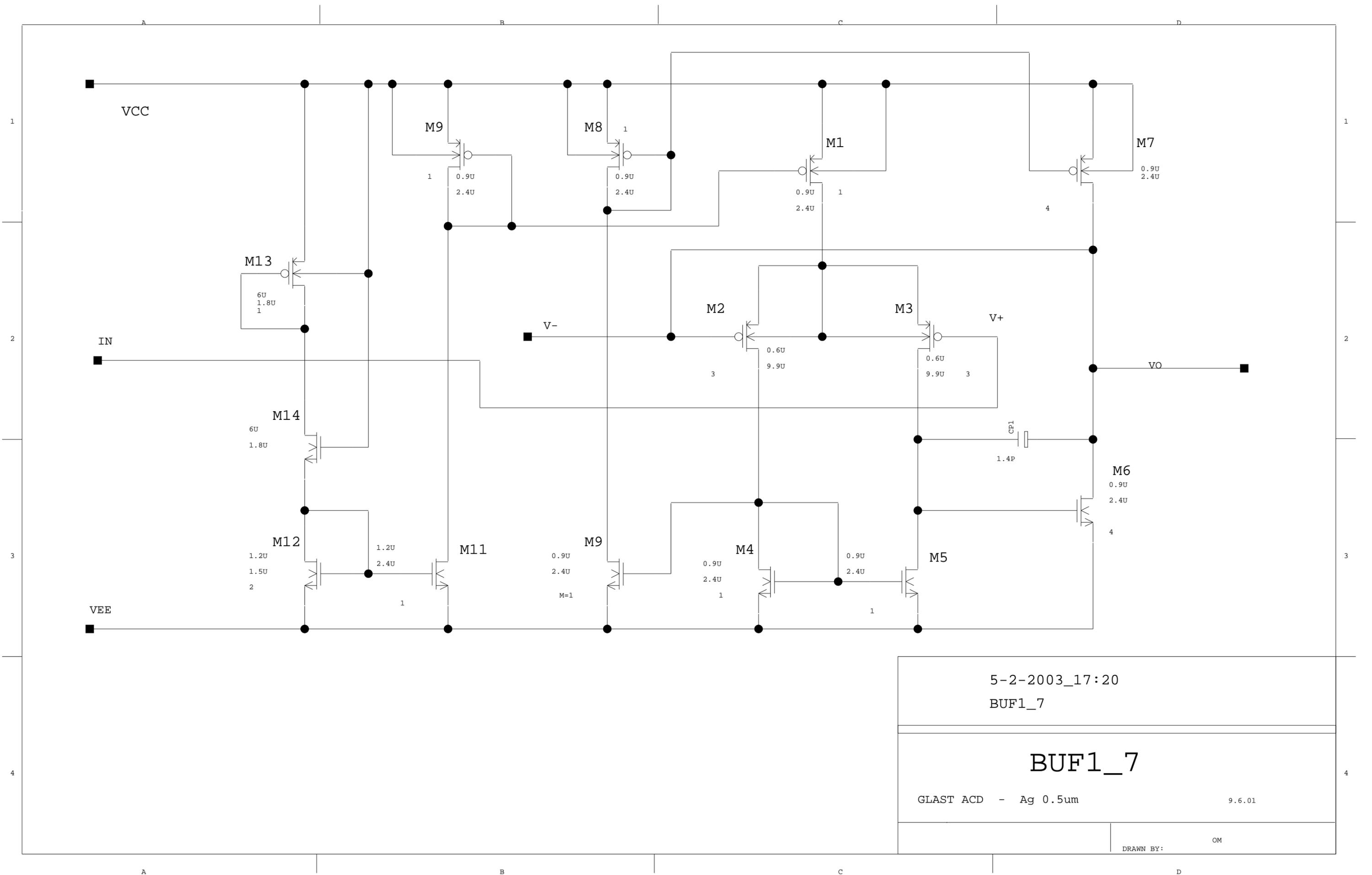


gcfe4: MN15 M=4, MP31 M=4 -> I=14u
gcfe2: MN15 M=3, MP31 M=2 -> I=6u
gcfe3: same as gcfe2

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DATE	APPROVALS	

SHEET 2 OF
orcvrfe7 5-14-2003_21:31





5-2-2003_17:20

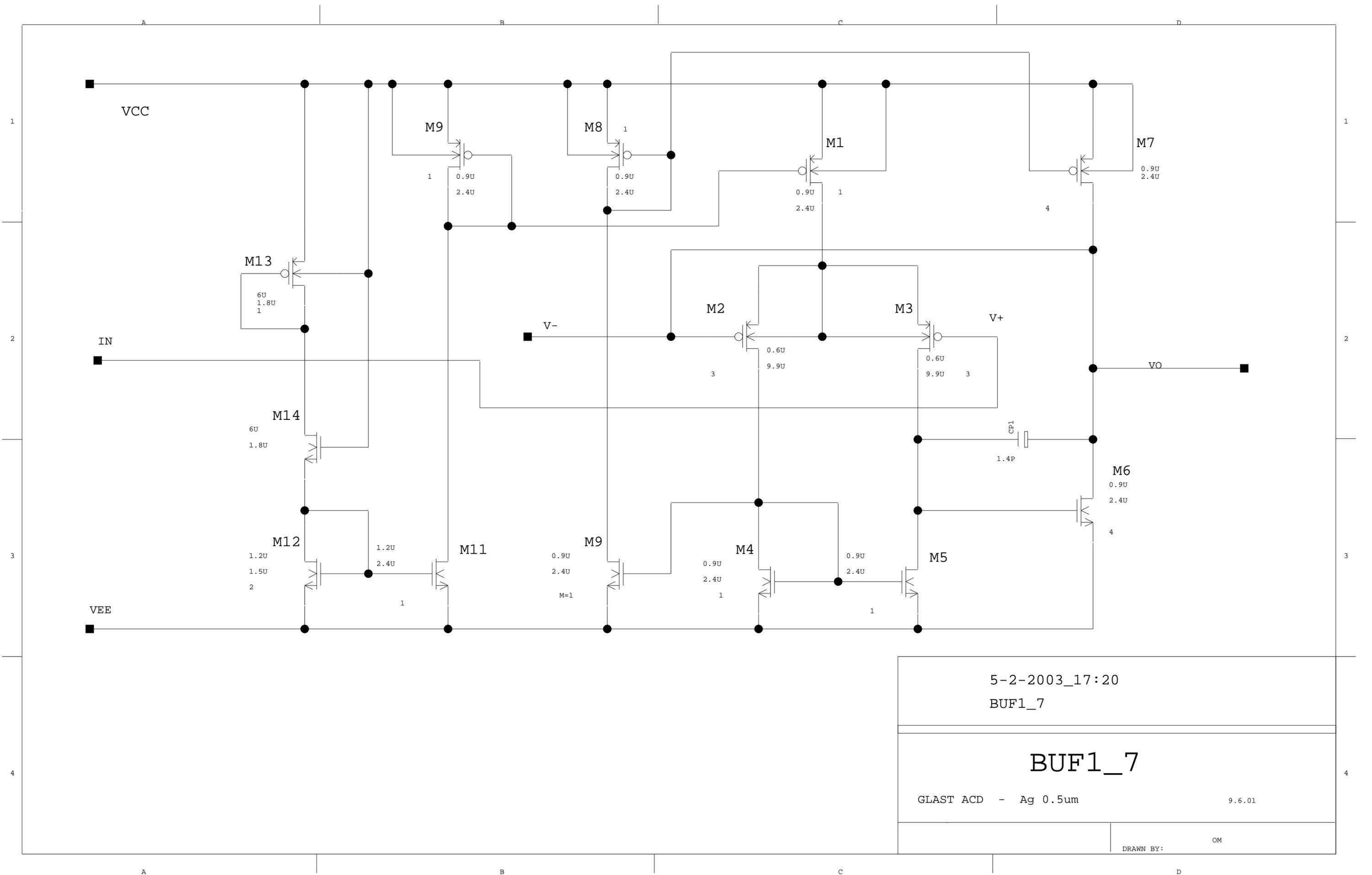
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BUF1_7

GLAST ACD - Ag 0.5um

9.6.01

DRAWN BY: OM



5-2-2003_17:20

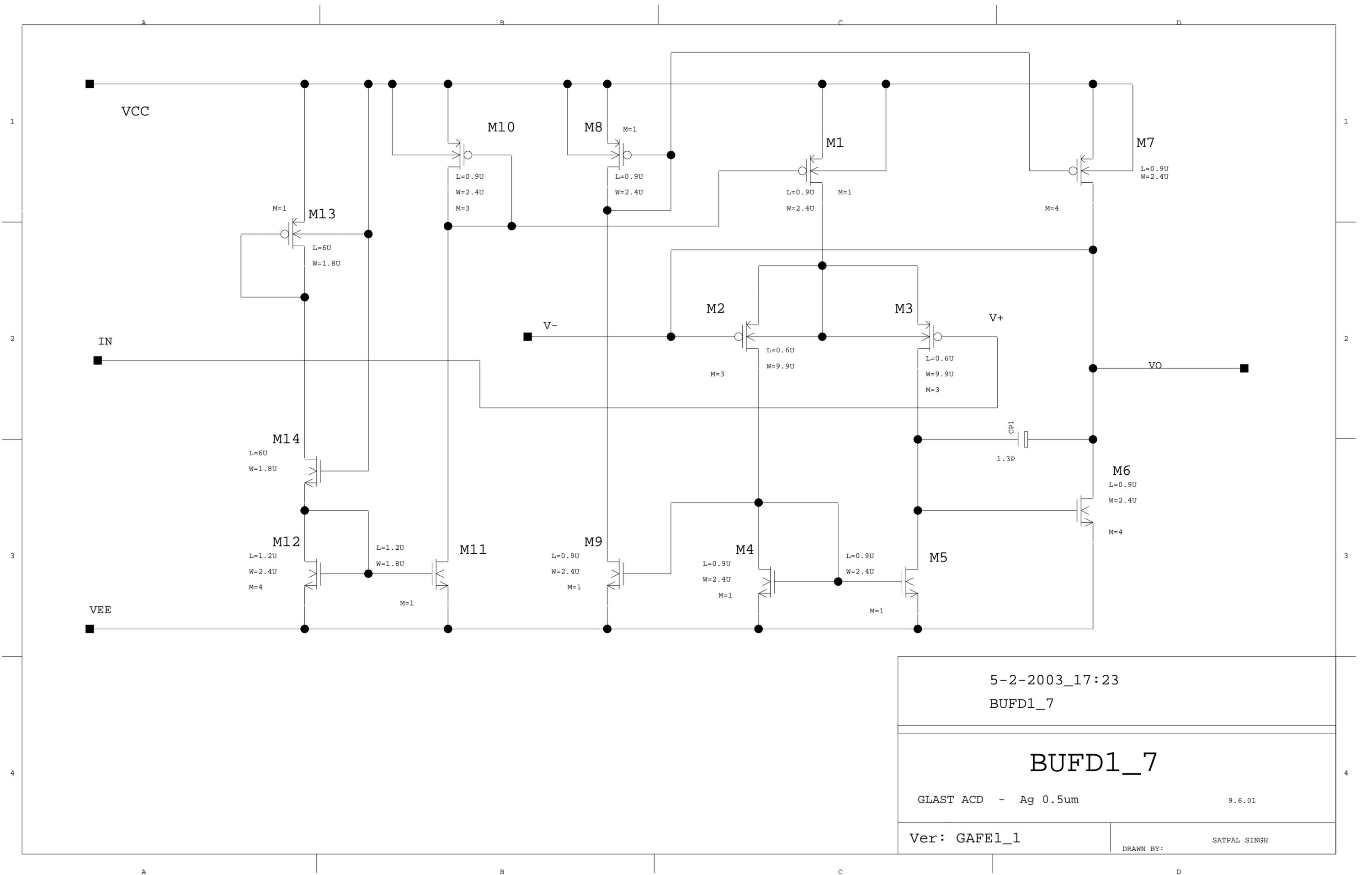
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9.6.01

DRAWN BY: OM



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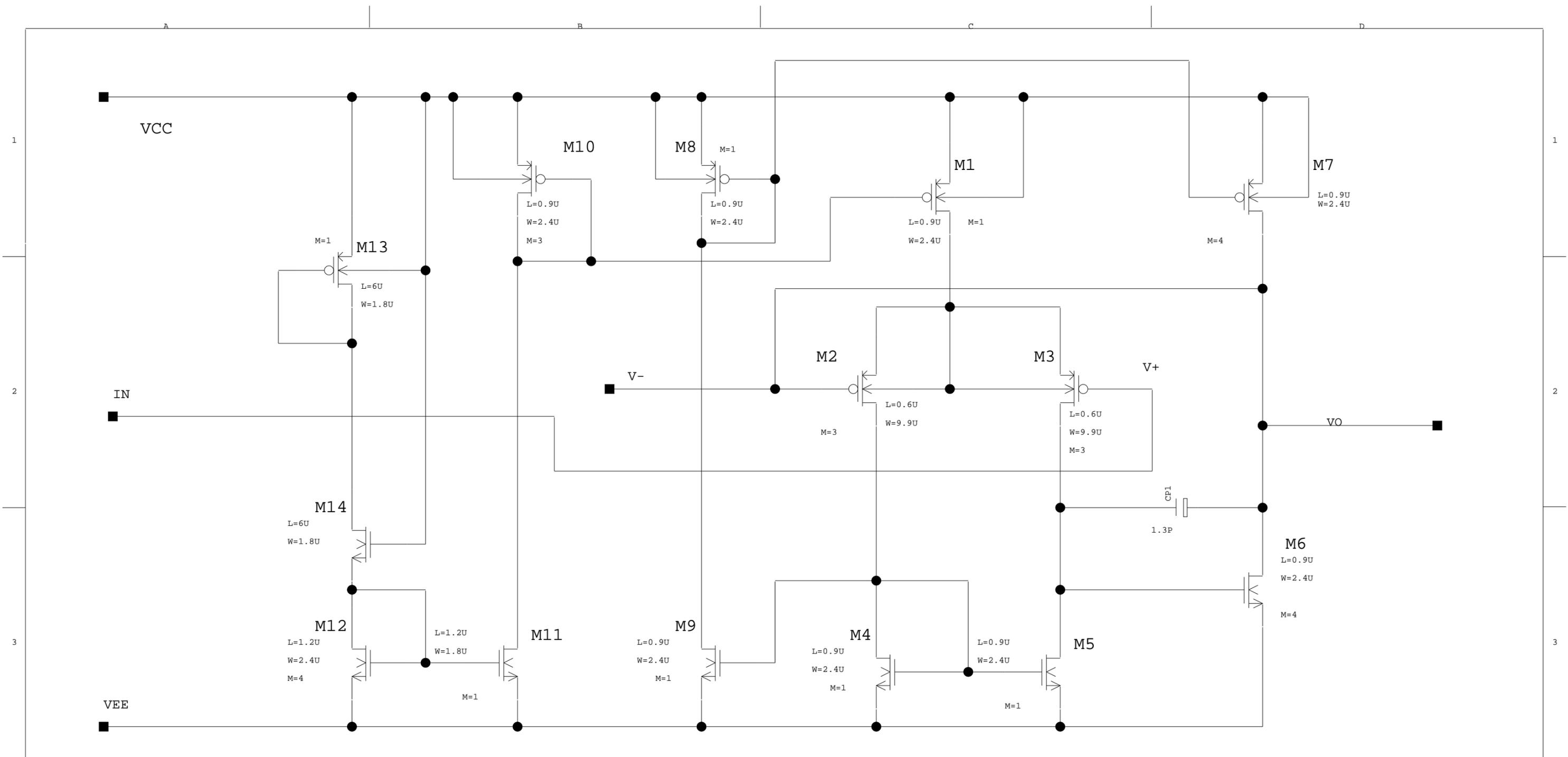
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9.6.01

Ver: GAFE1_1

DRAWN BY:

SATPAL SINGH



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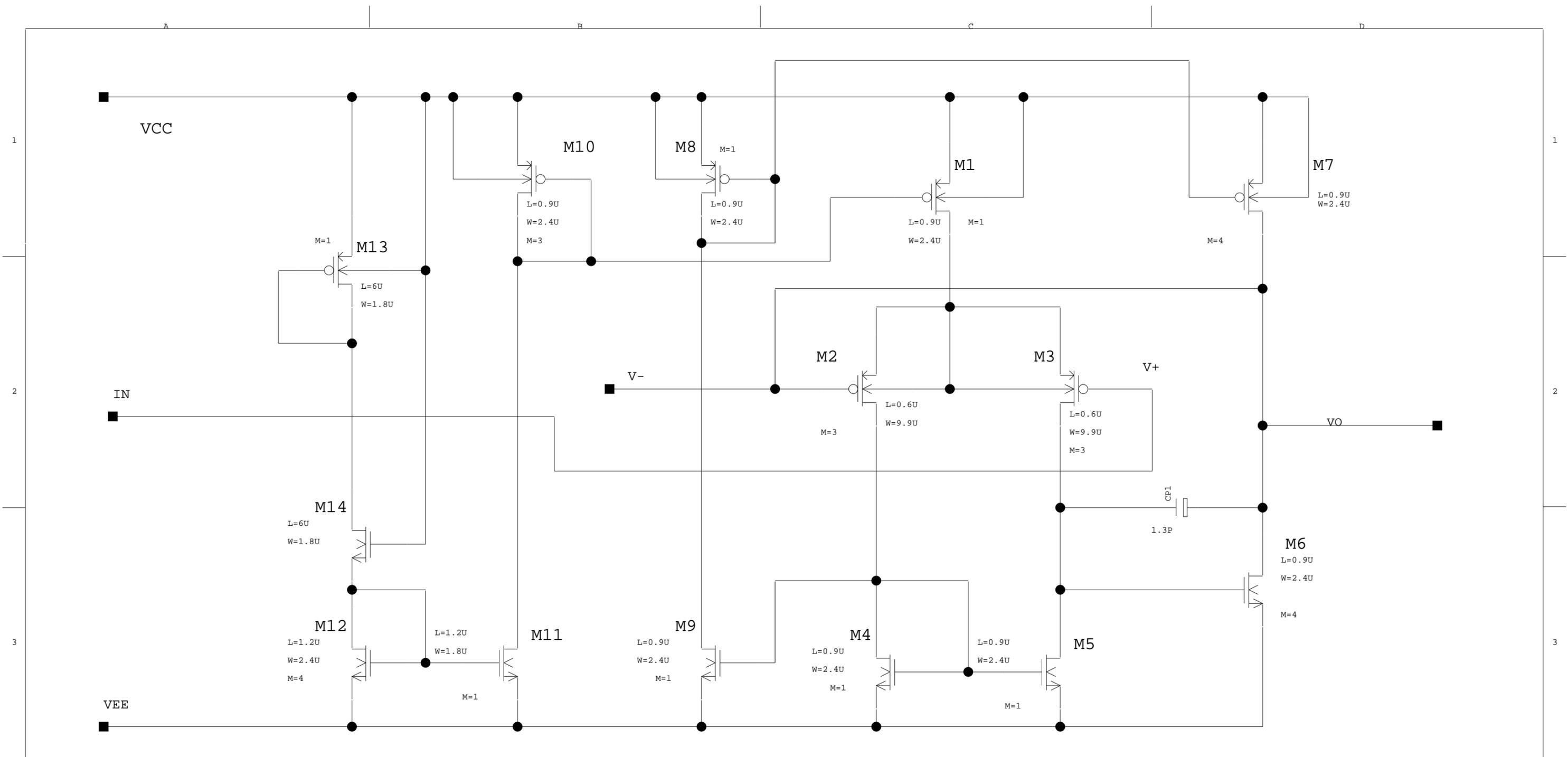
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Ver: GAFE1_1

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SATPAL SINGH



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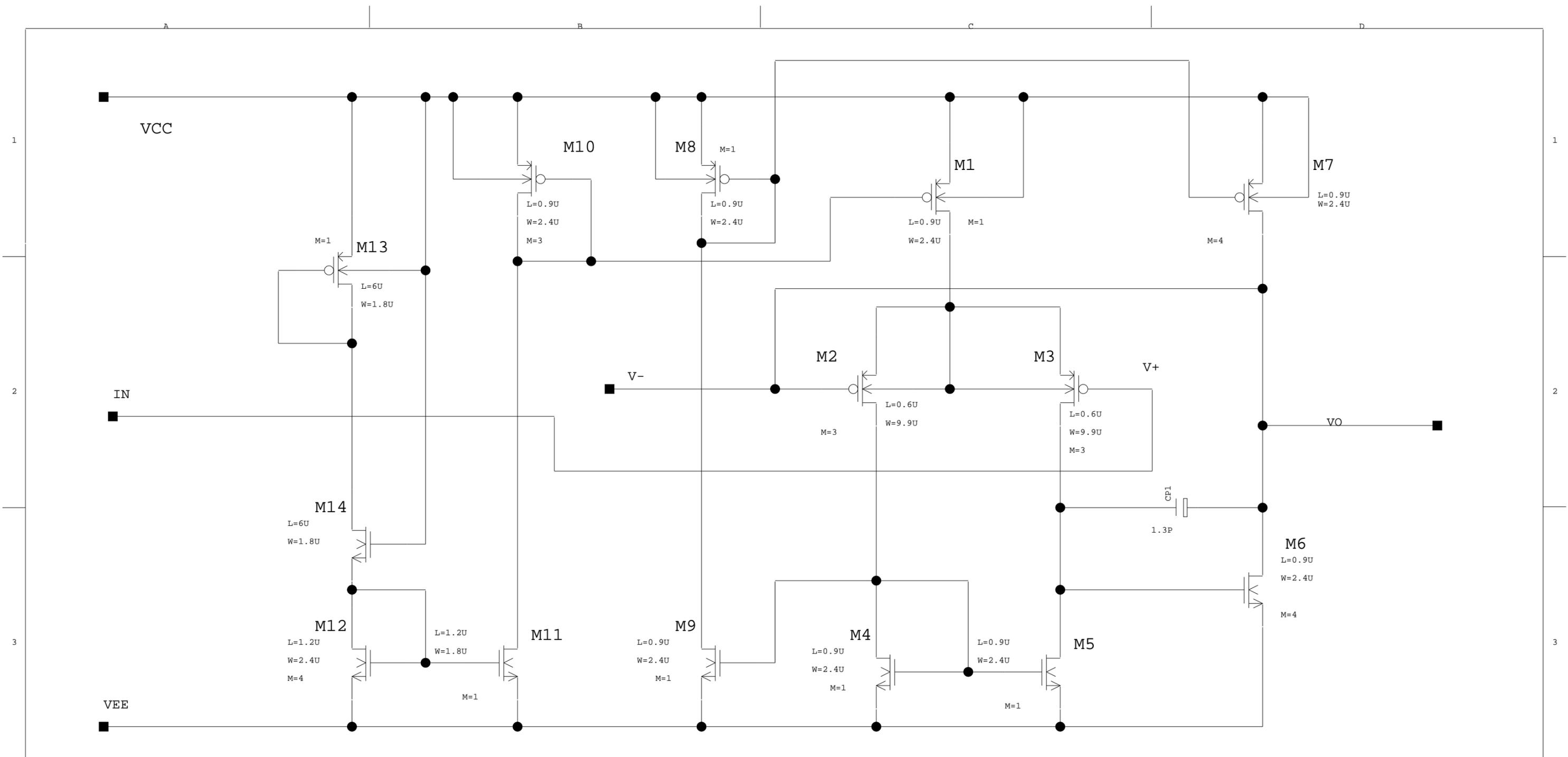
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Ver: GAFE1_1

DRAWN BY:

SATPAL SINGH



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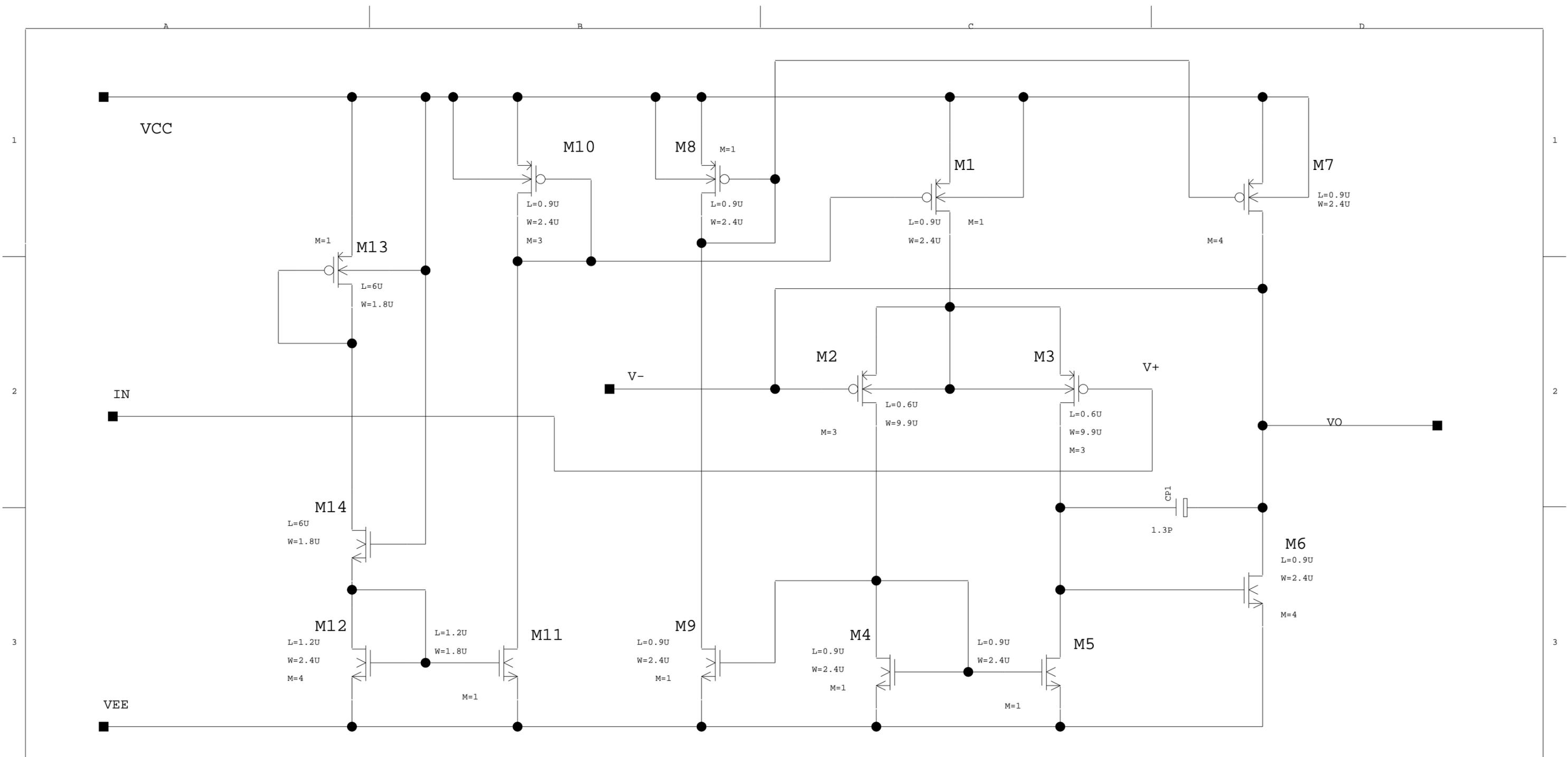
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Ver: GAFE1_1

DRAWN BY:

SATPAL SINGH



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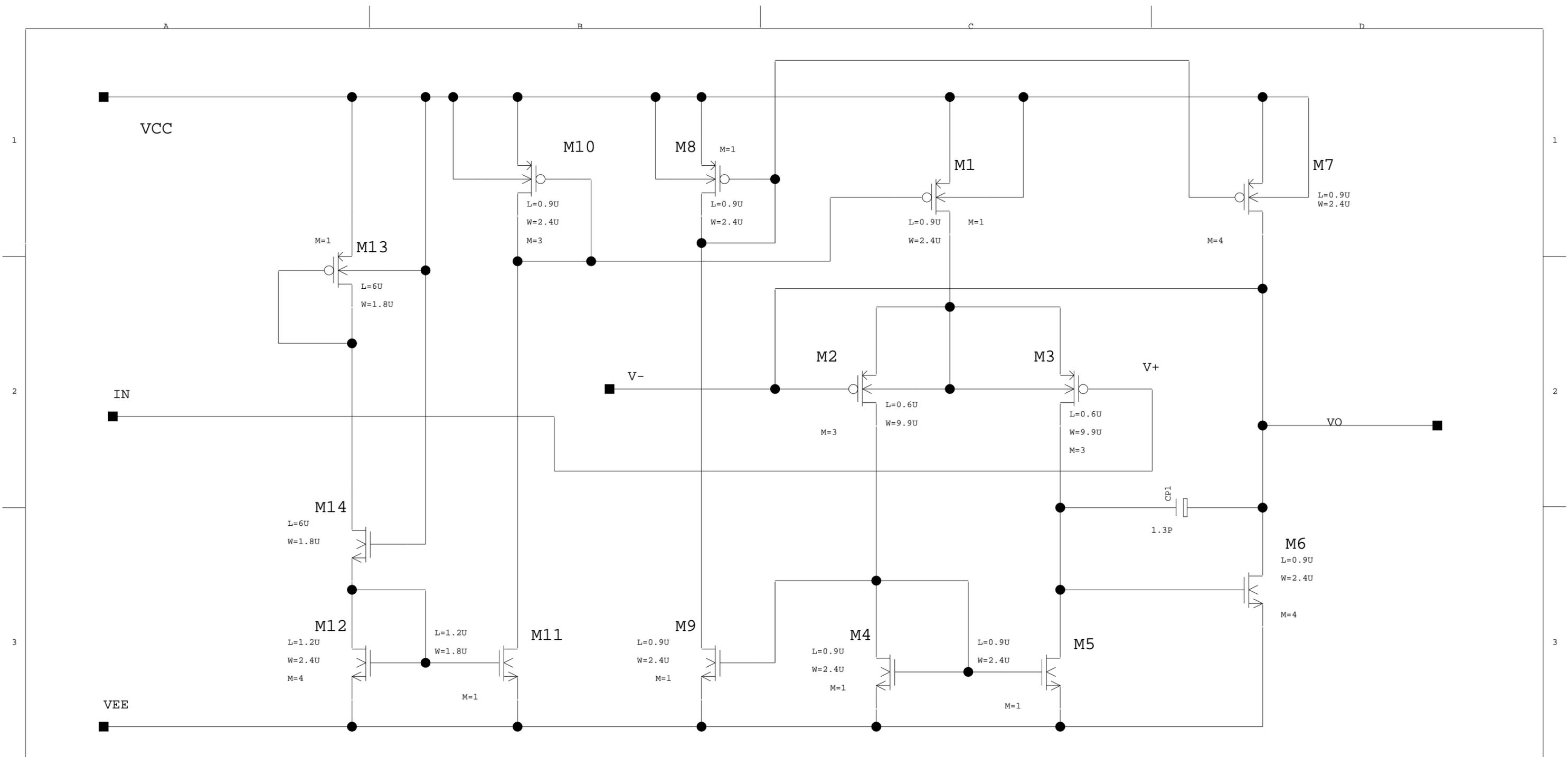
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Ver: GAFE1_1

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SATPAL SINGH



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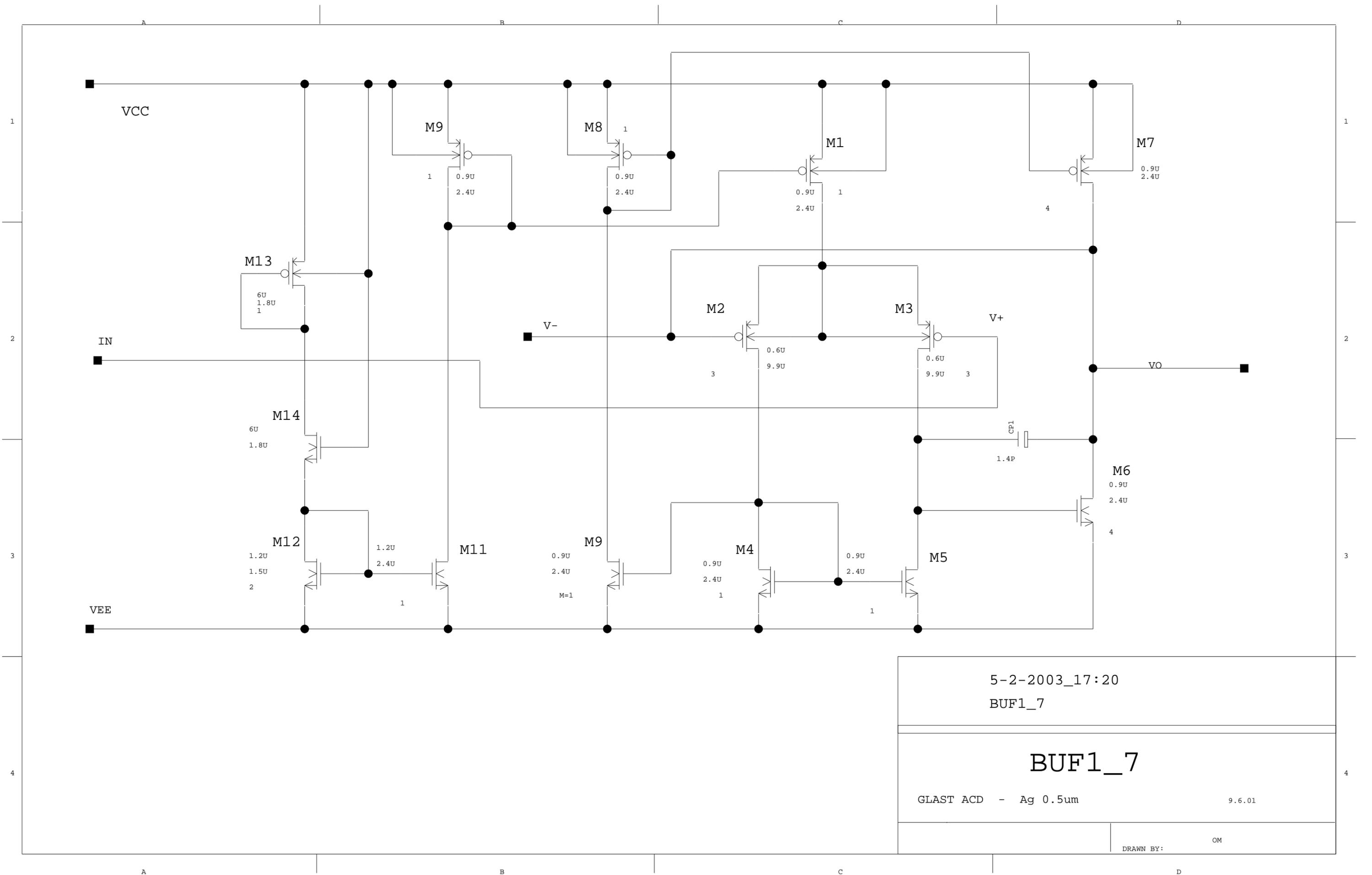
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9.6.01

Ver: GAFE1_1

DRAWN BY: SATPAL SINGH



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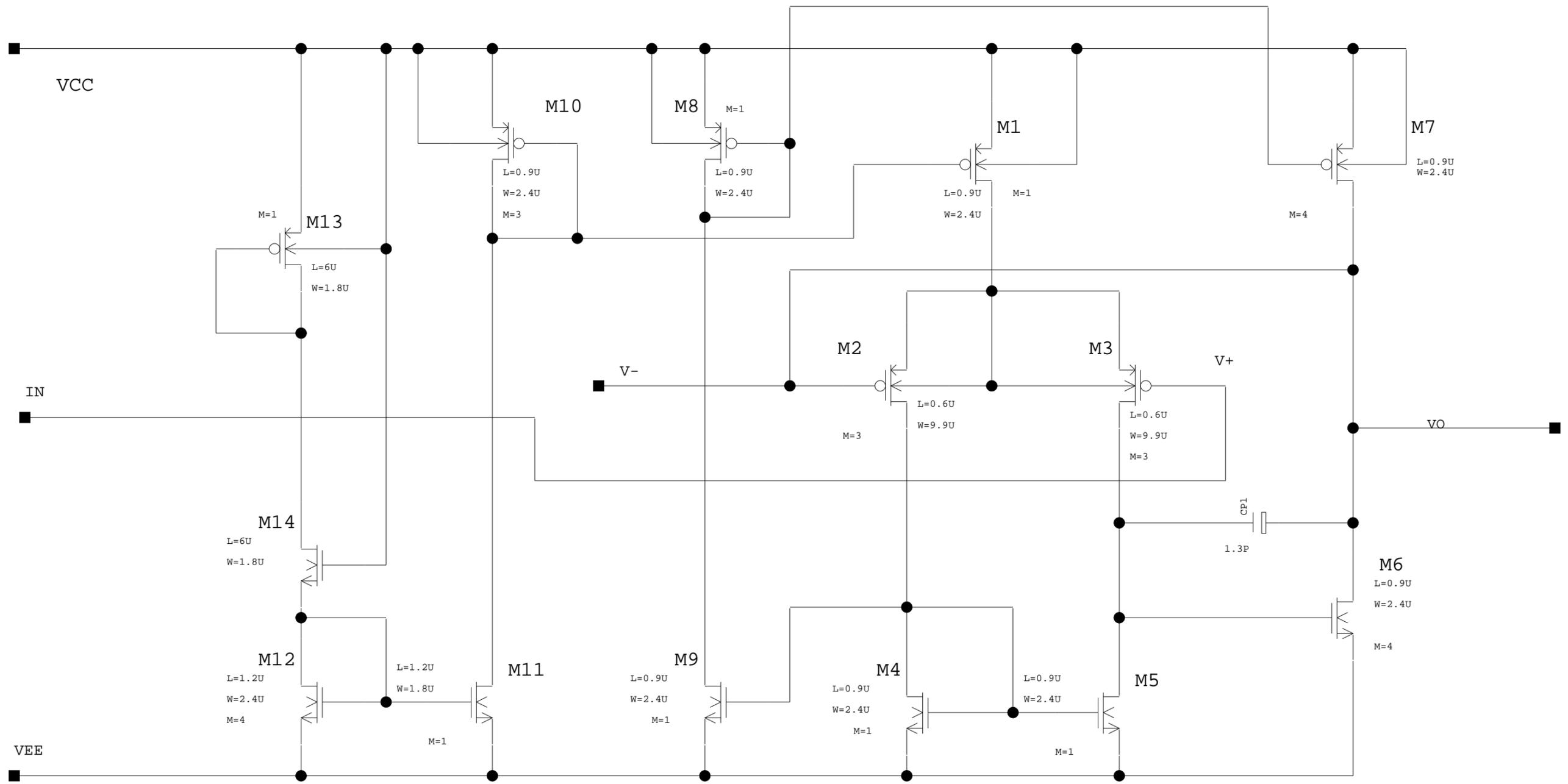
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BUF1_7

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9.6.01

DRAWN BY: OM



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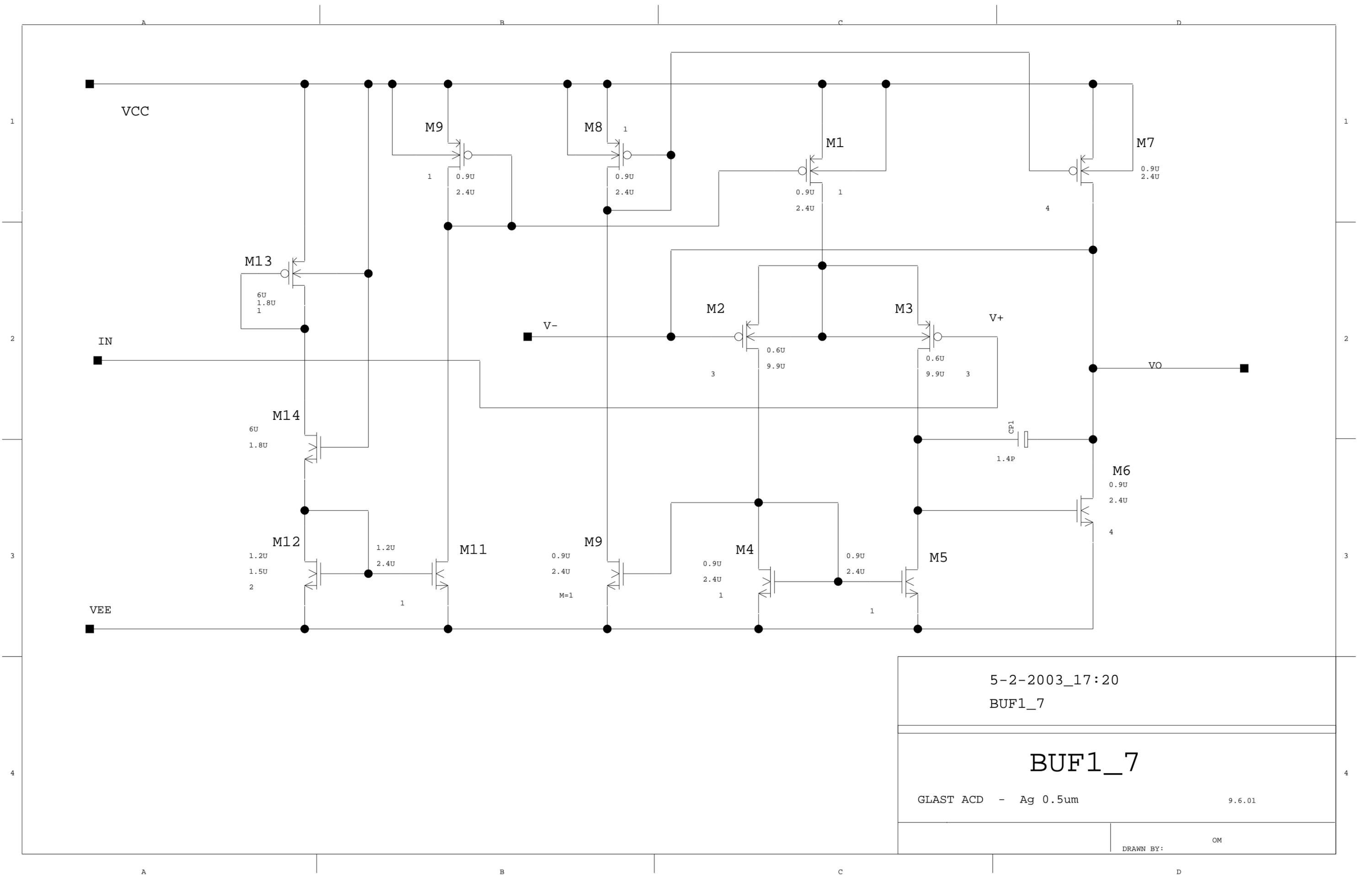
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9.6.01

Ver: GAFE1_1

DRAWN BY:

SATPAL SINGH



5-2-2003_17:20

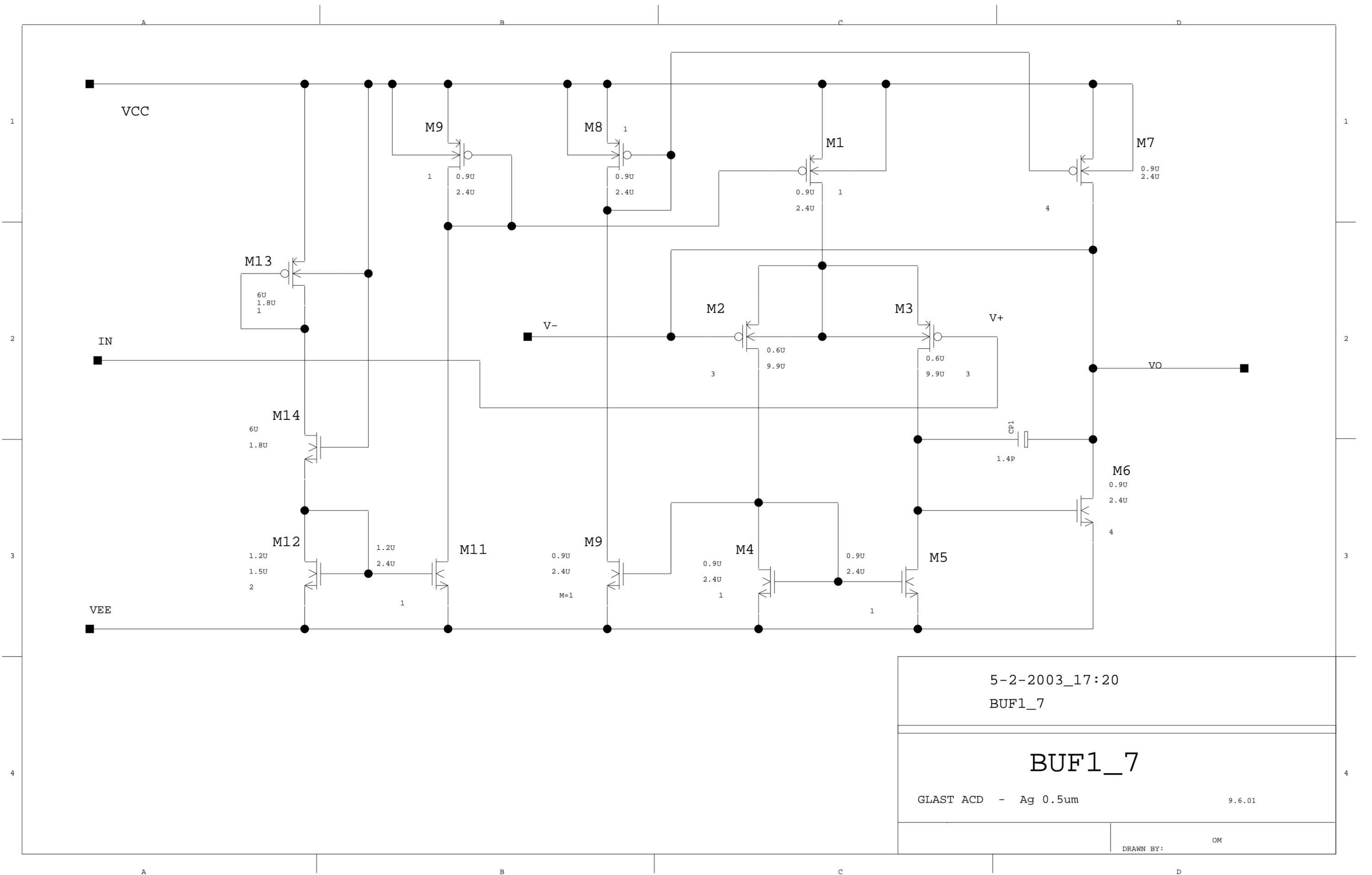
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BUF1_7

GLAST ACD - Ag 0.5um

9.6.01

DRAWN BY: OM



5-2-2003_17:20

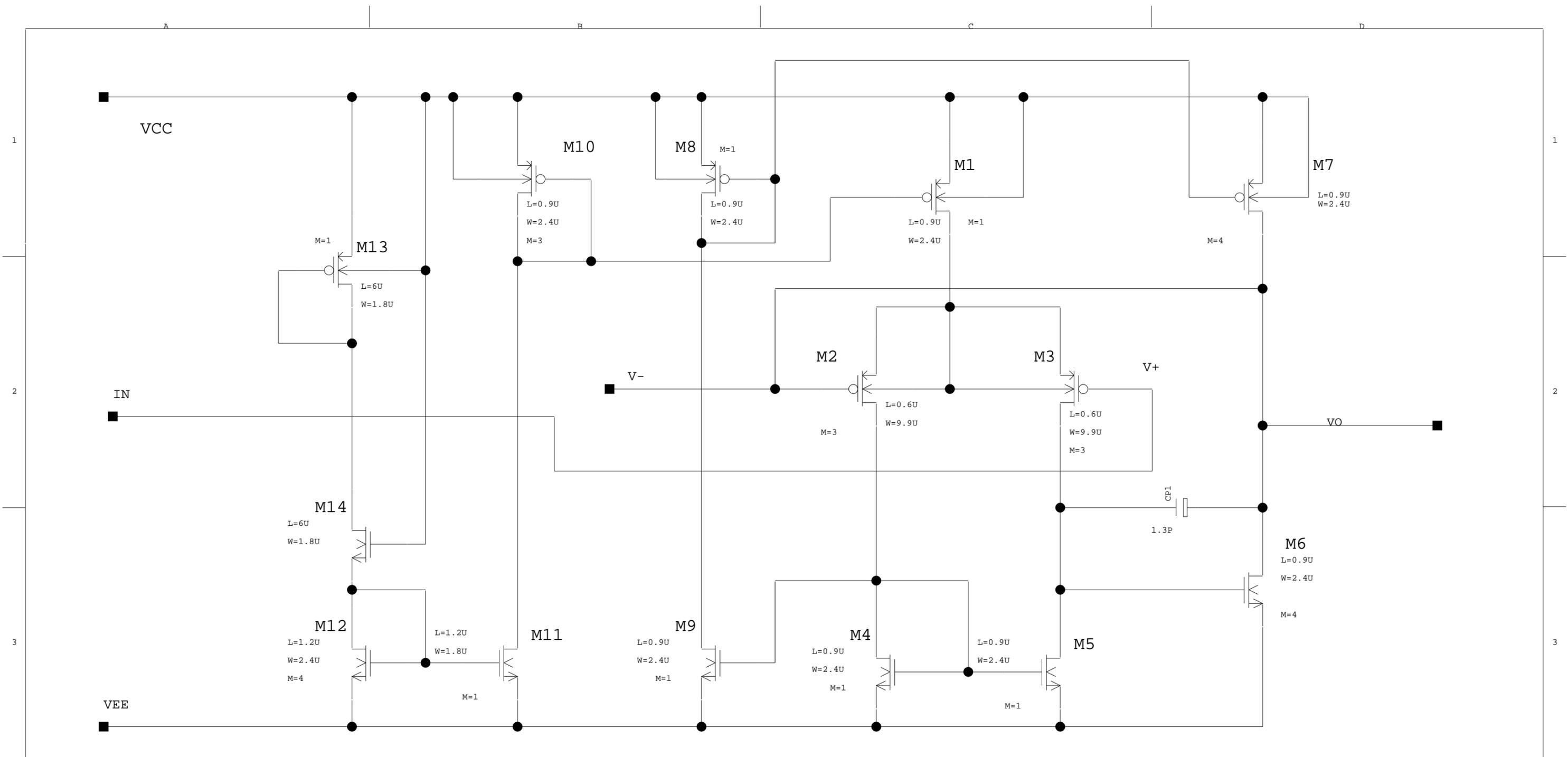
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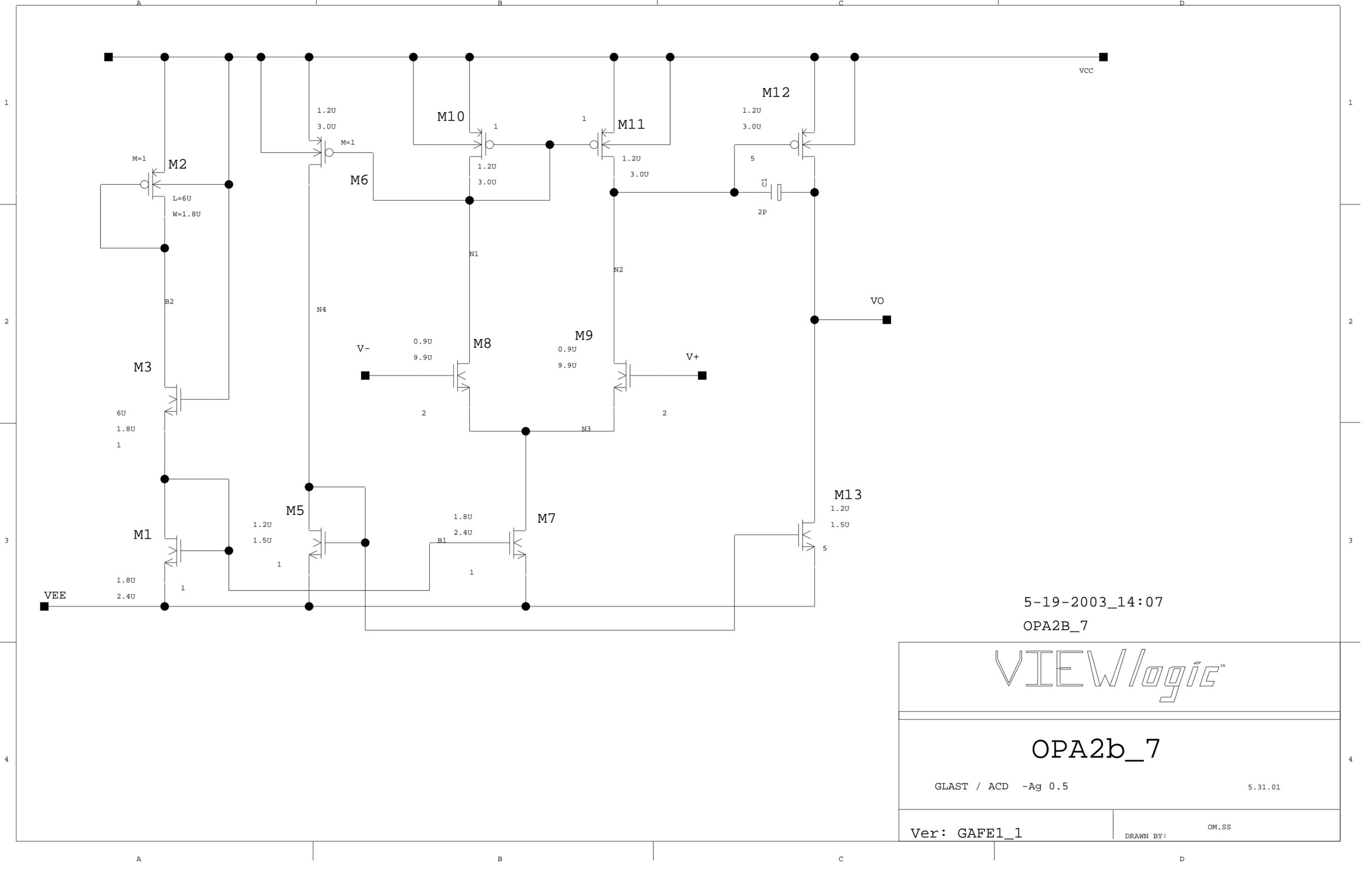
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9.6.01

Ver: GAFE1_1

DRAWN BY:

SATPAL SINGH



5-19-2003_14:07
 OPA2B_7

VIEWlogic™

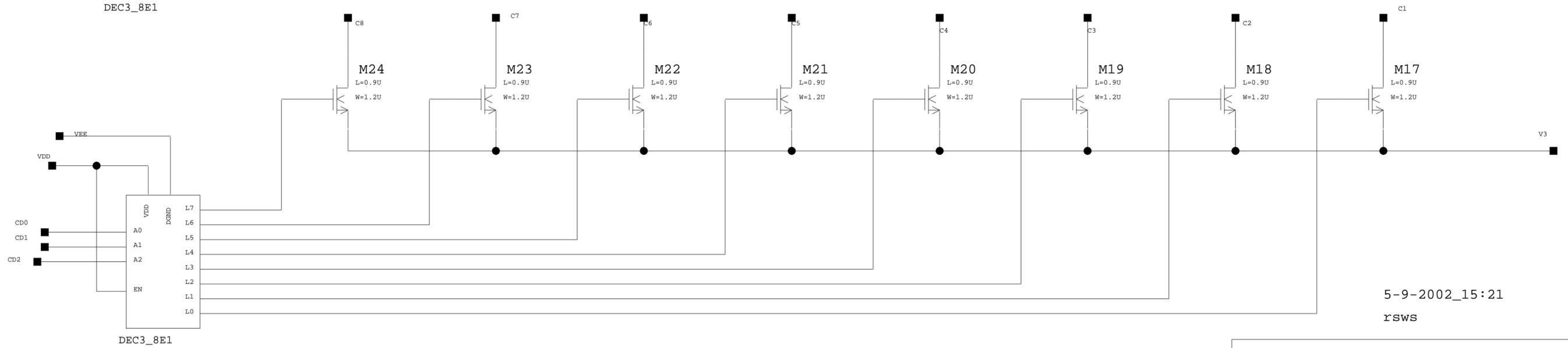
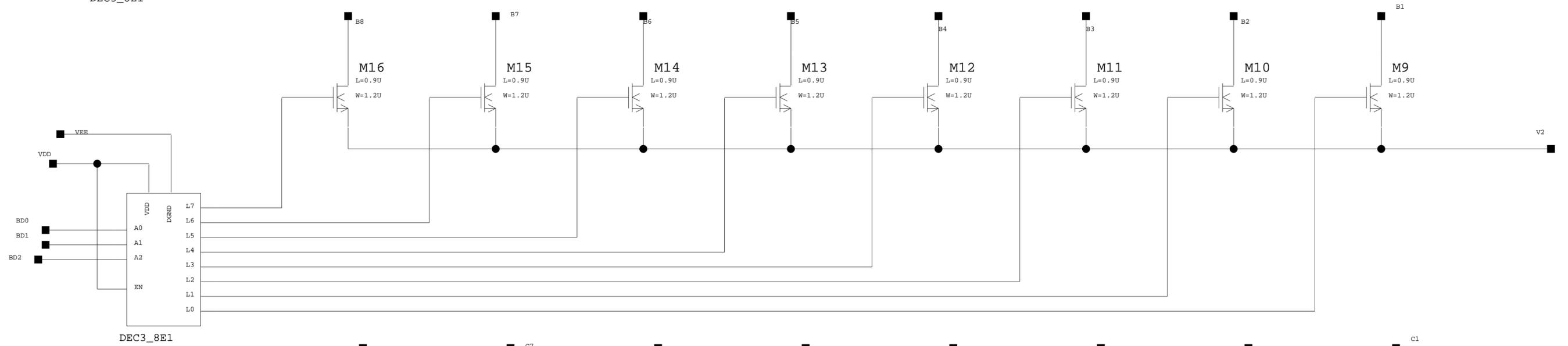
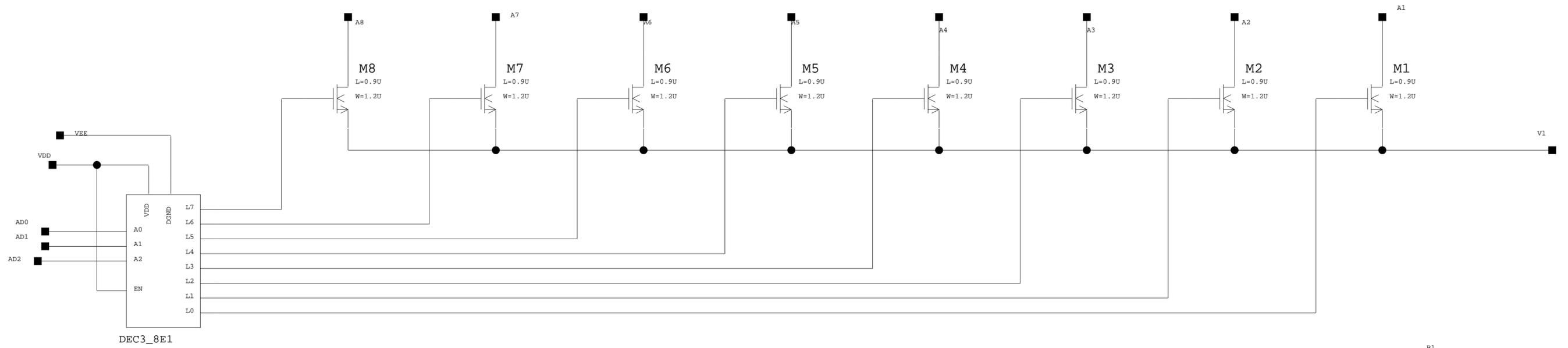
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GLAST / ACD -Ag 0.5

5.31.01

Ver: GAFE1_1

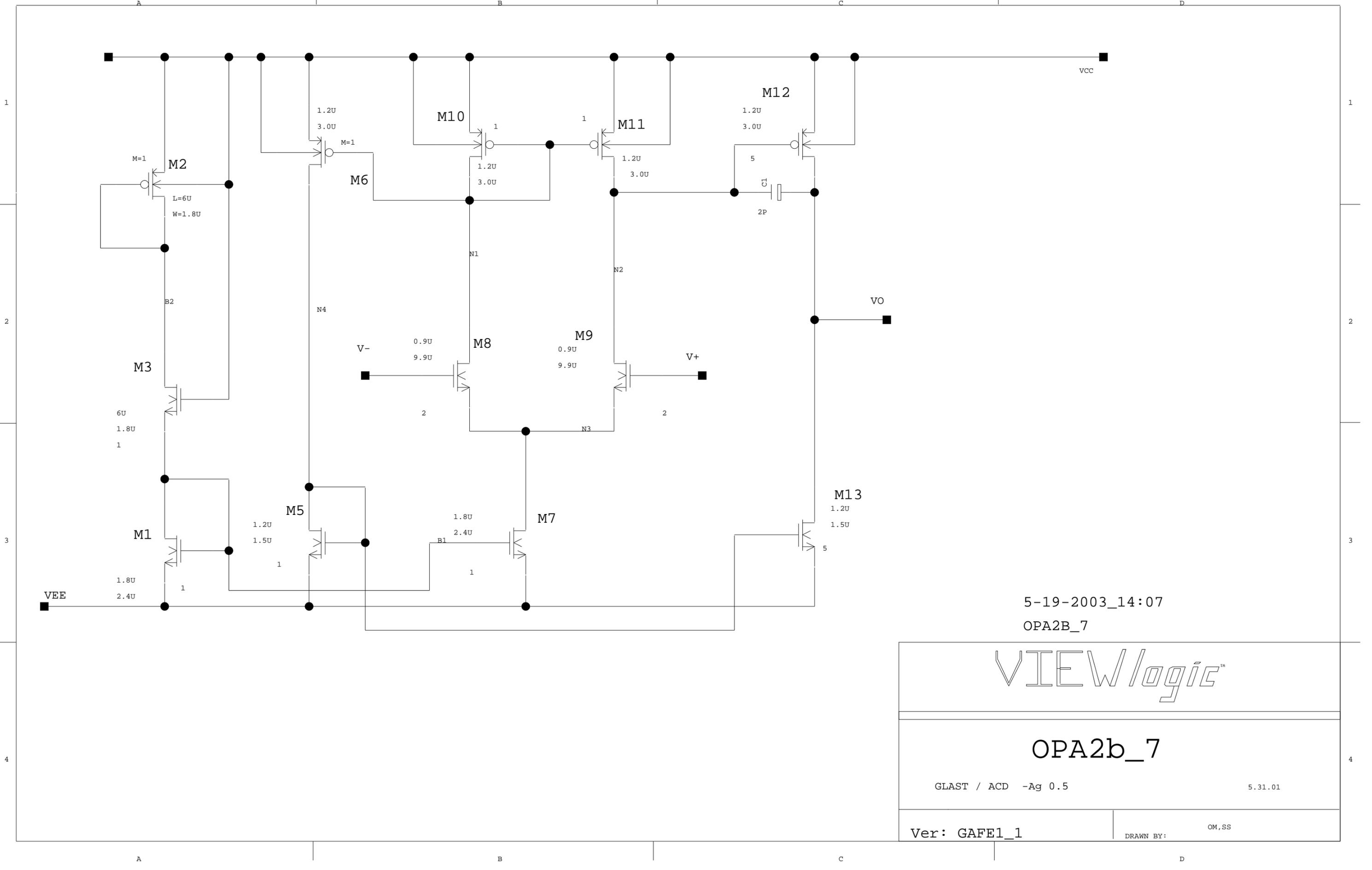
DRAWN BY: OM,SS



5-9-2002_15:21

RSWS

<h1>LHEA - NASA</h1>	
RSWS	3.6.02
Proj: GLAST ACD	
ver: GAFB1_1	DRAWN BY: Satpal Singh



5-19-2003_14:07
 OPA2B_7

VIEWlogic™

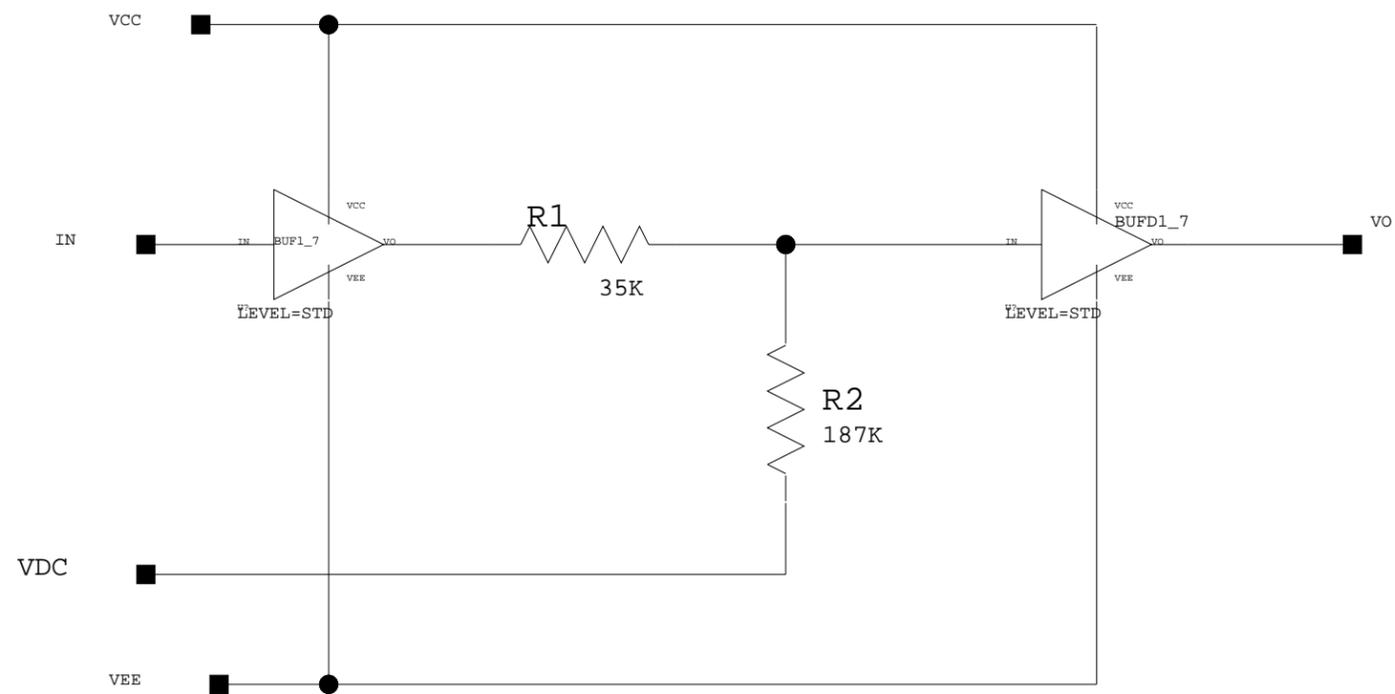
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GLAST / ACD -Ag 0.5

5.31.01

Ver: GAFE1_1

DRAWN BY: OM,SS



5-19-2003_13:59

HAMP7

LHEA - NASA

HAMP7

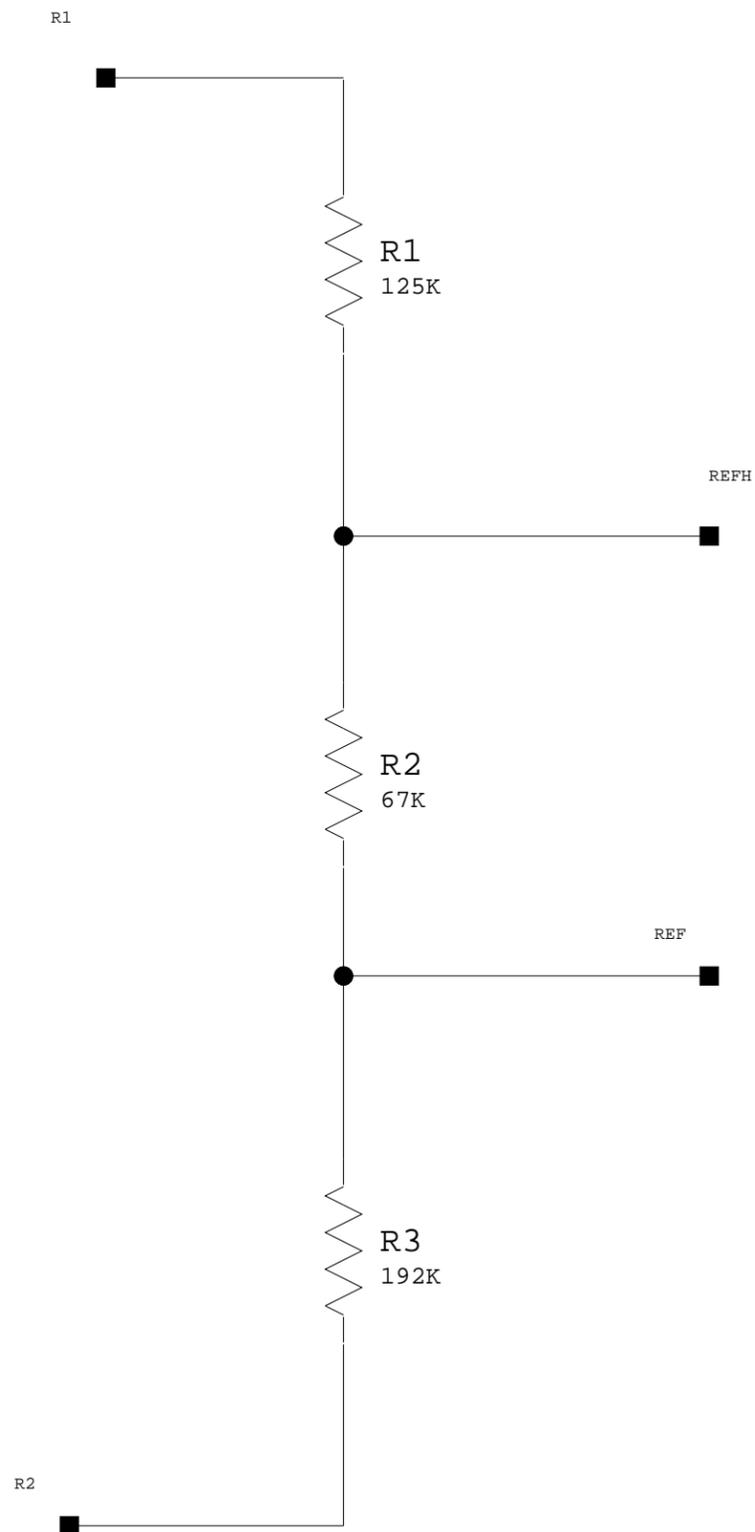
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Proj: GLAST ACD

ver: GAFE1_1

DRAWN BY:

Satpal Singh



5-12-2003_14:11
rblk2_7

LHEA - NASA

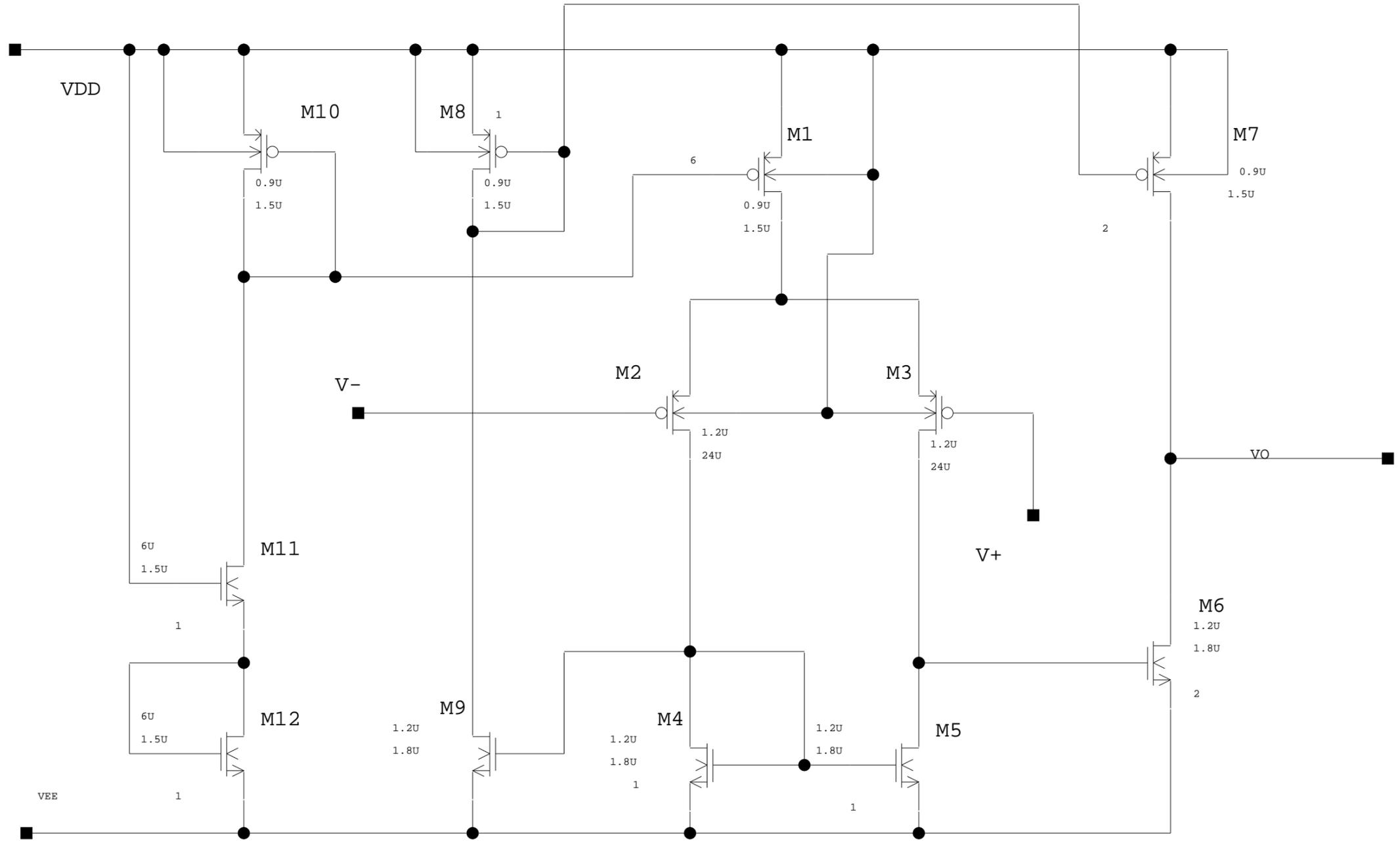
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ver: GAFE1_1

DRAWN BY:

Satpal Singh



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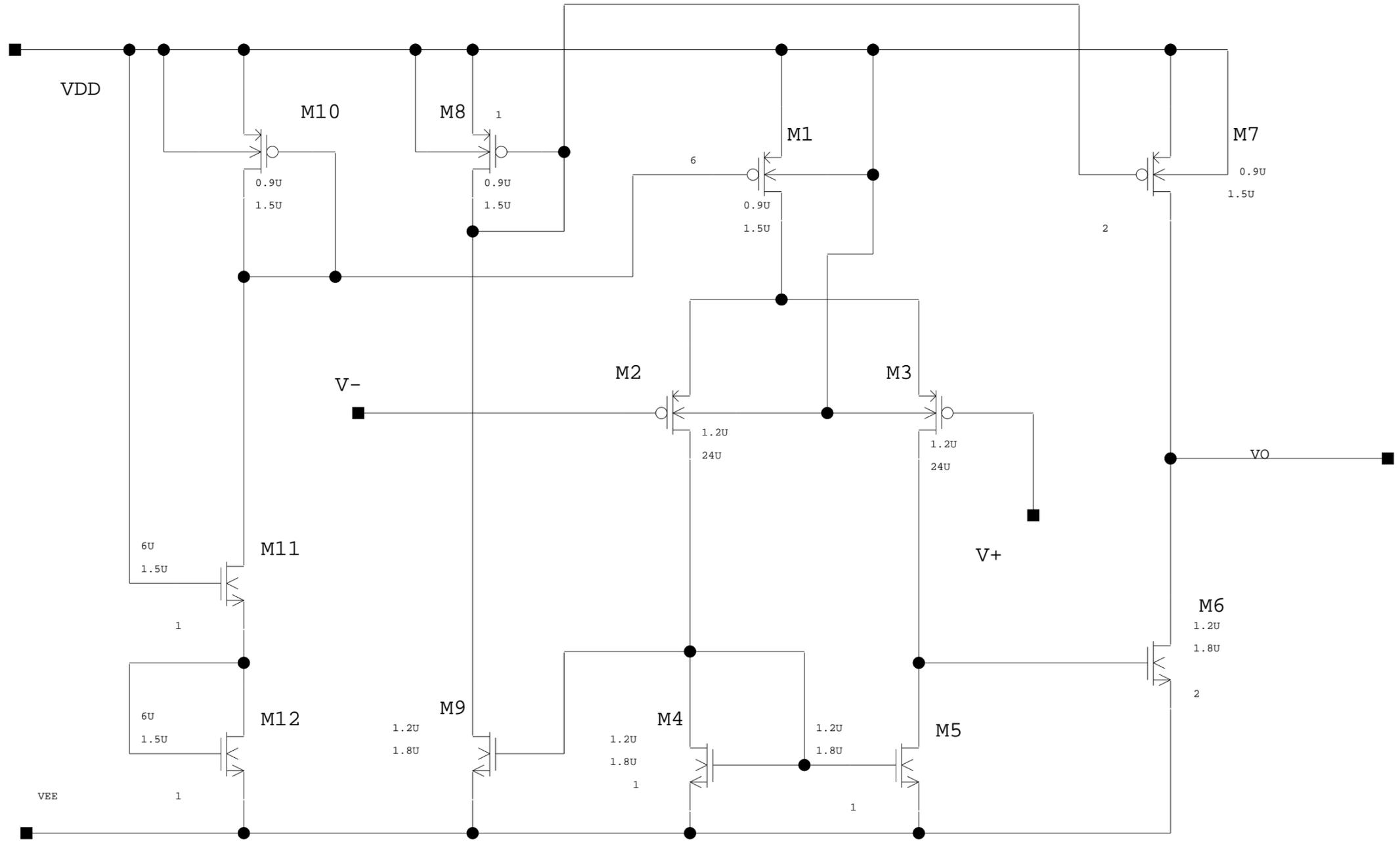
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2.1.02

Ver: GAFE1_1

DRAWN BY: SS



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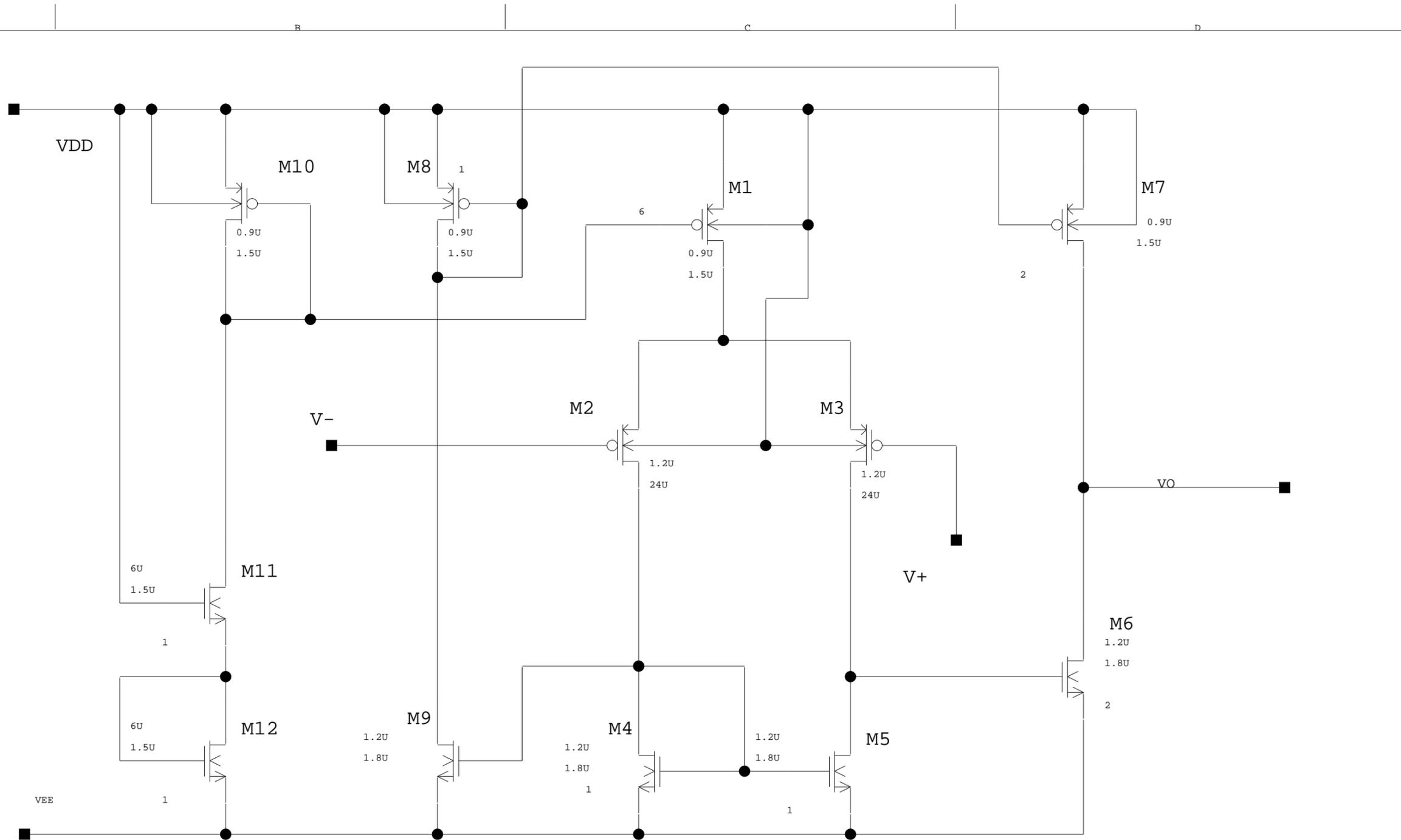
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2.1.02

Ver: GAFE1_1

DRAWN BY: SS



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opap1f7

OPAP1F7

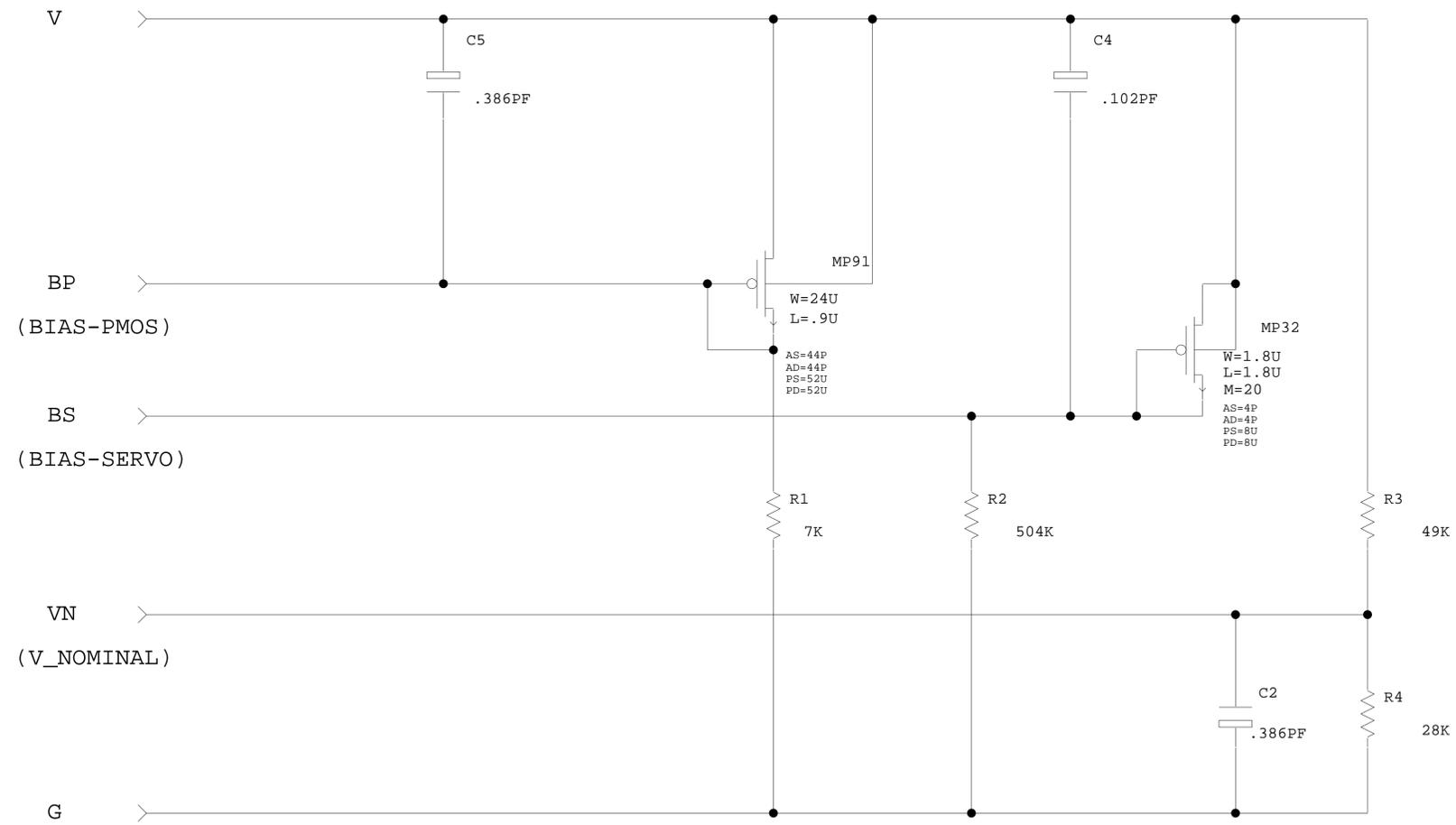
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Ver: GAFE1_1

DRAWN BY:

SS



1l_bias

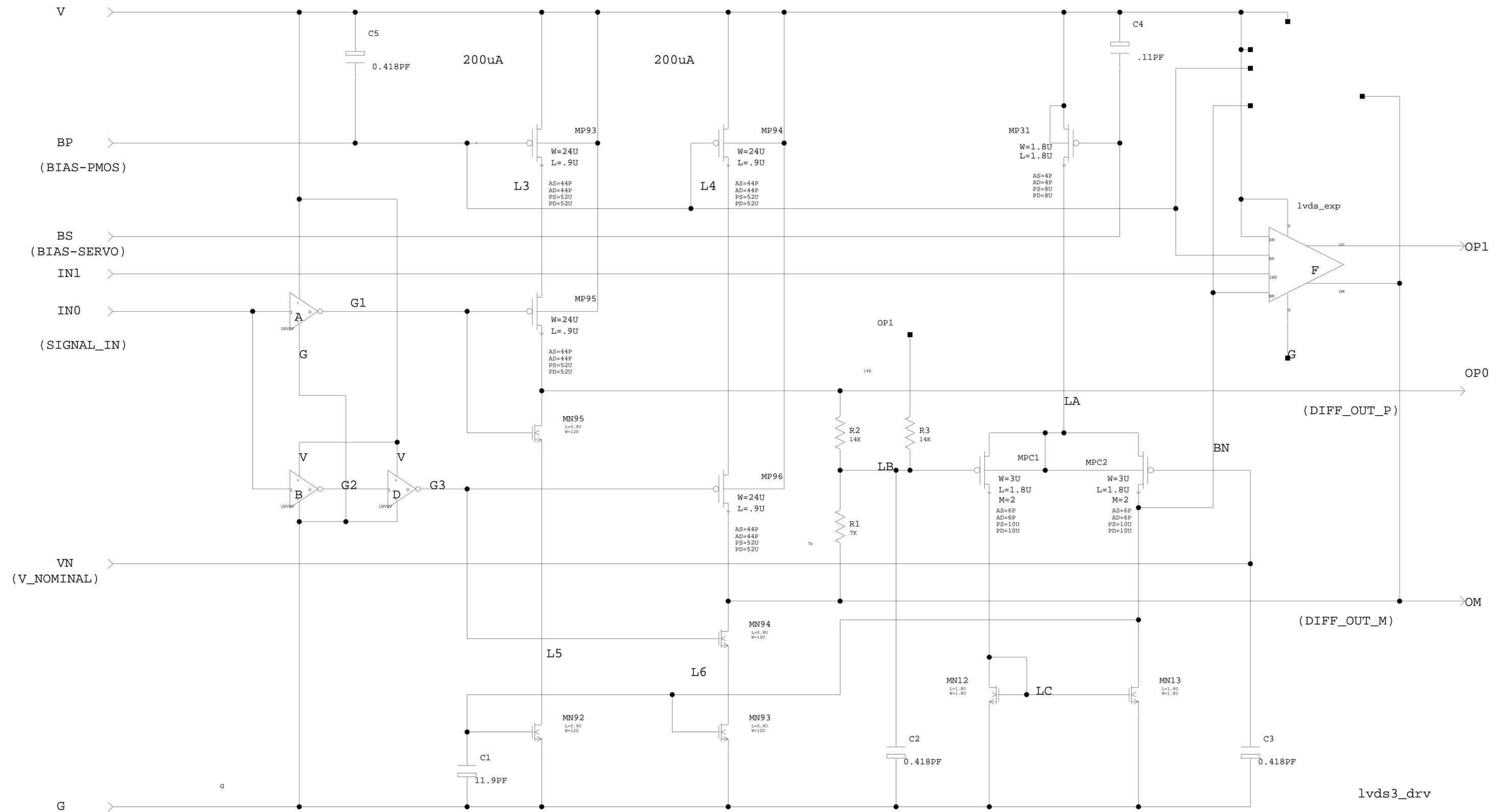
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ENGR	DATE	APPROVALS
DFTB		
CHKD		

SHEET OF

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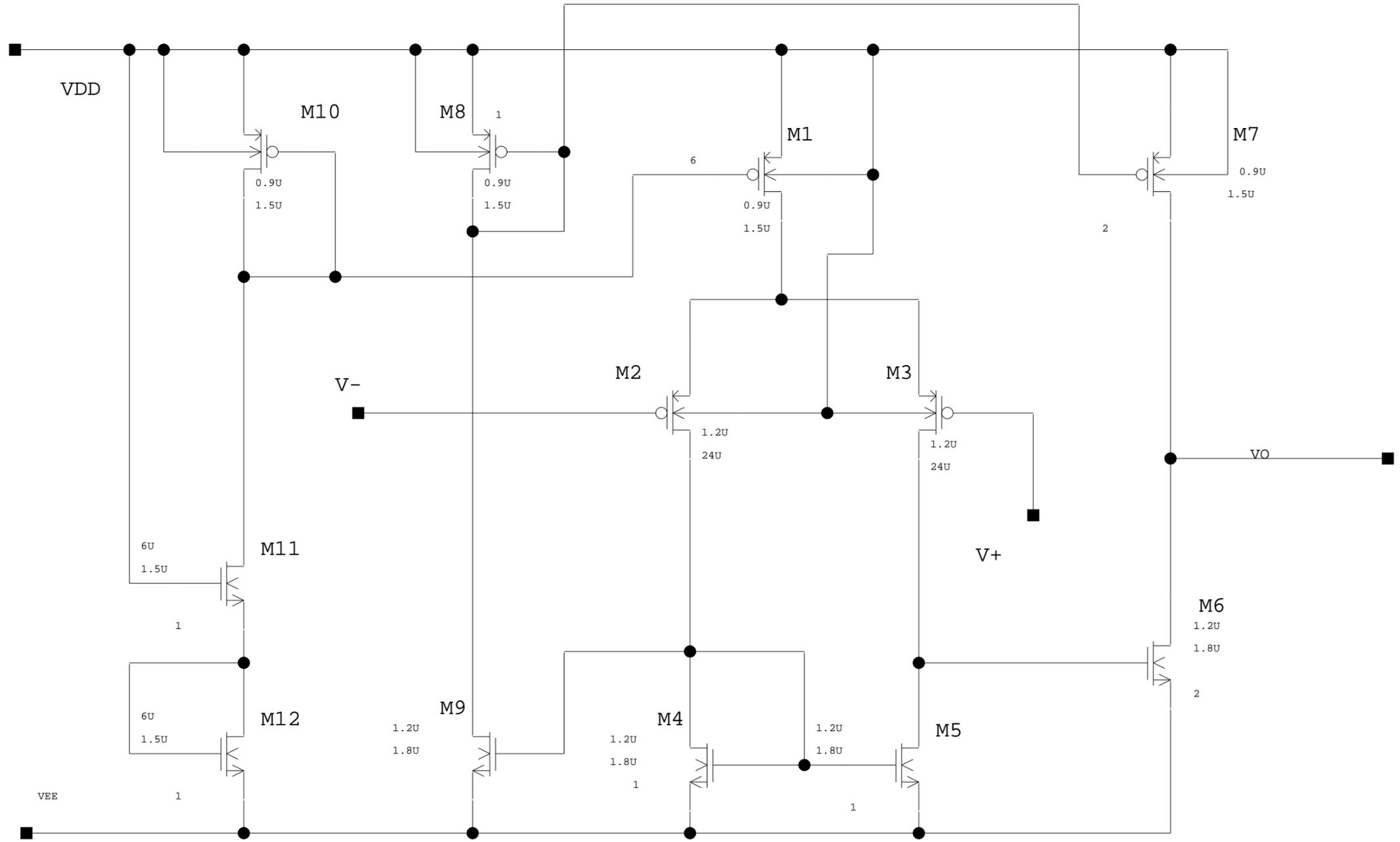
Servo Amplifier



lvds3_drv

9-17-2002_15:10

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ENGR	DATE	APPROVALS
DFTS		
CDRS		



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opap1f7

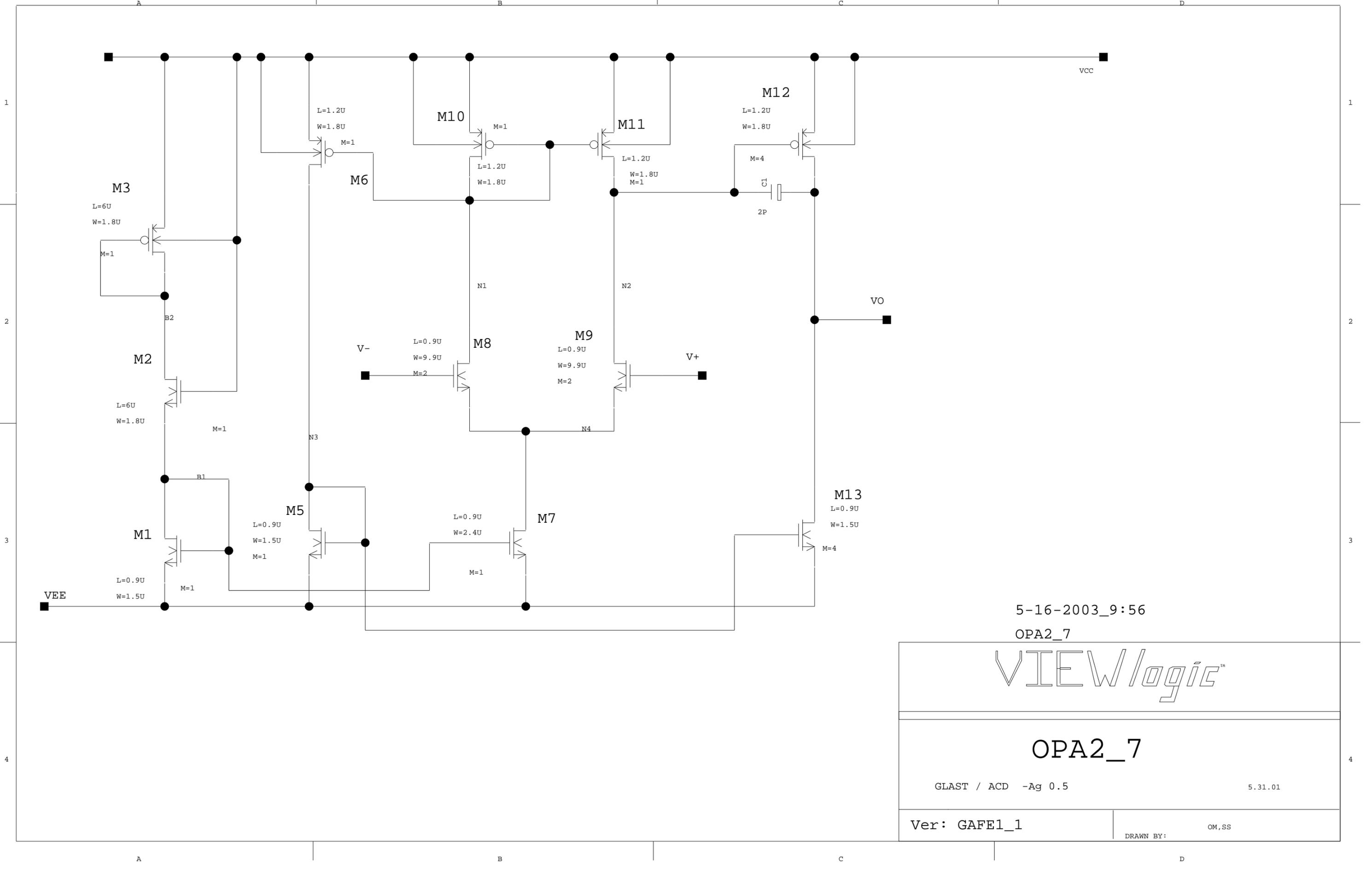
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GLAST ACD

2.1.02

Ver: GAFE1_1

DRAWN BY: SS



5-16-2003_9:56

OPA2_7

VIEWlogic™

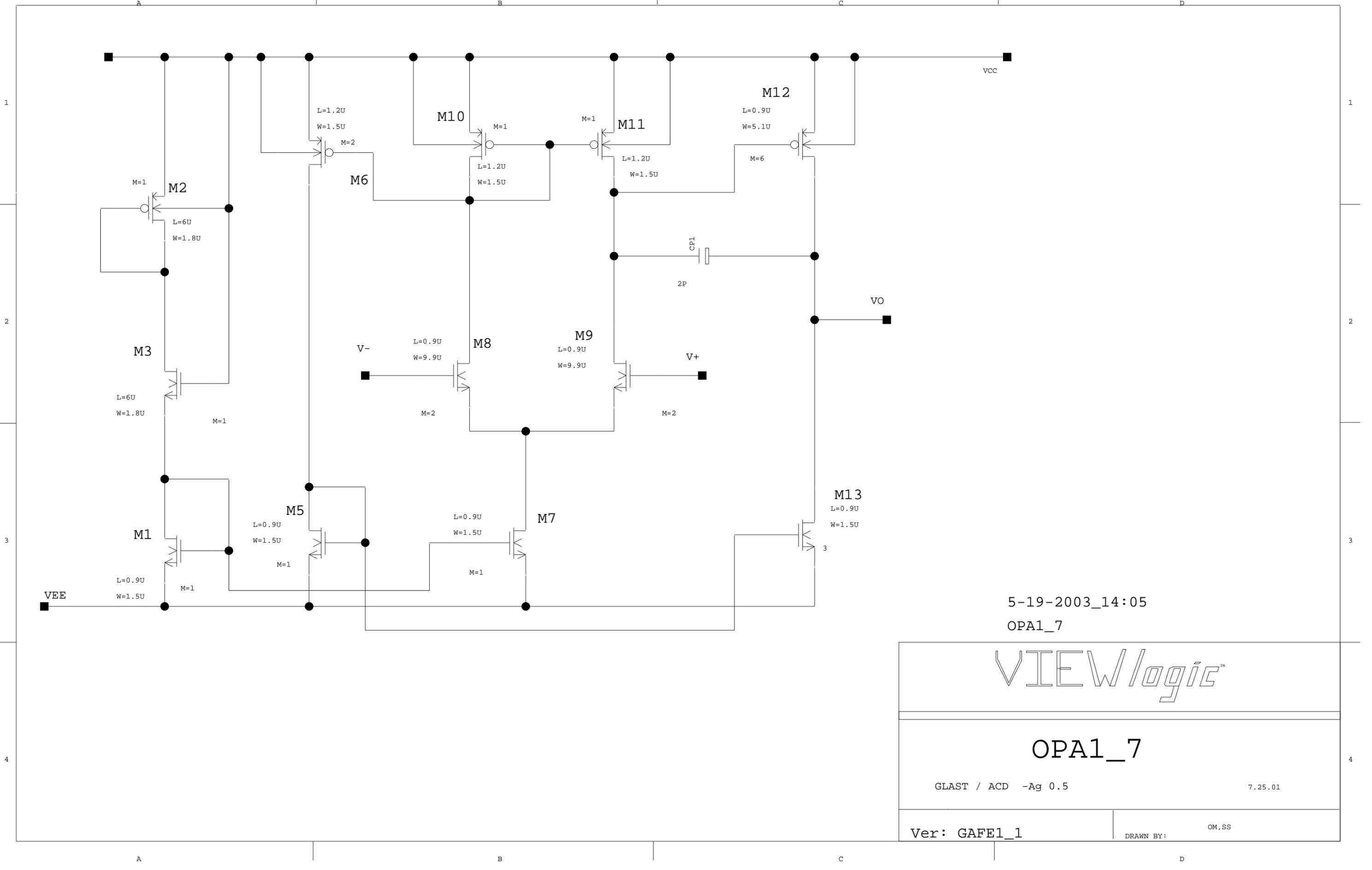
OPA2_7

GLAST / ACD -Ag 0.5

5.31.01

Ver: GAFE1_1

DRAWN BY: OM,SS



5-19-2003_14:05
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VIEWlogic™

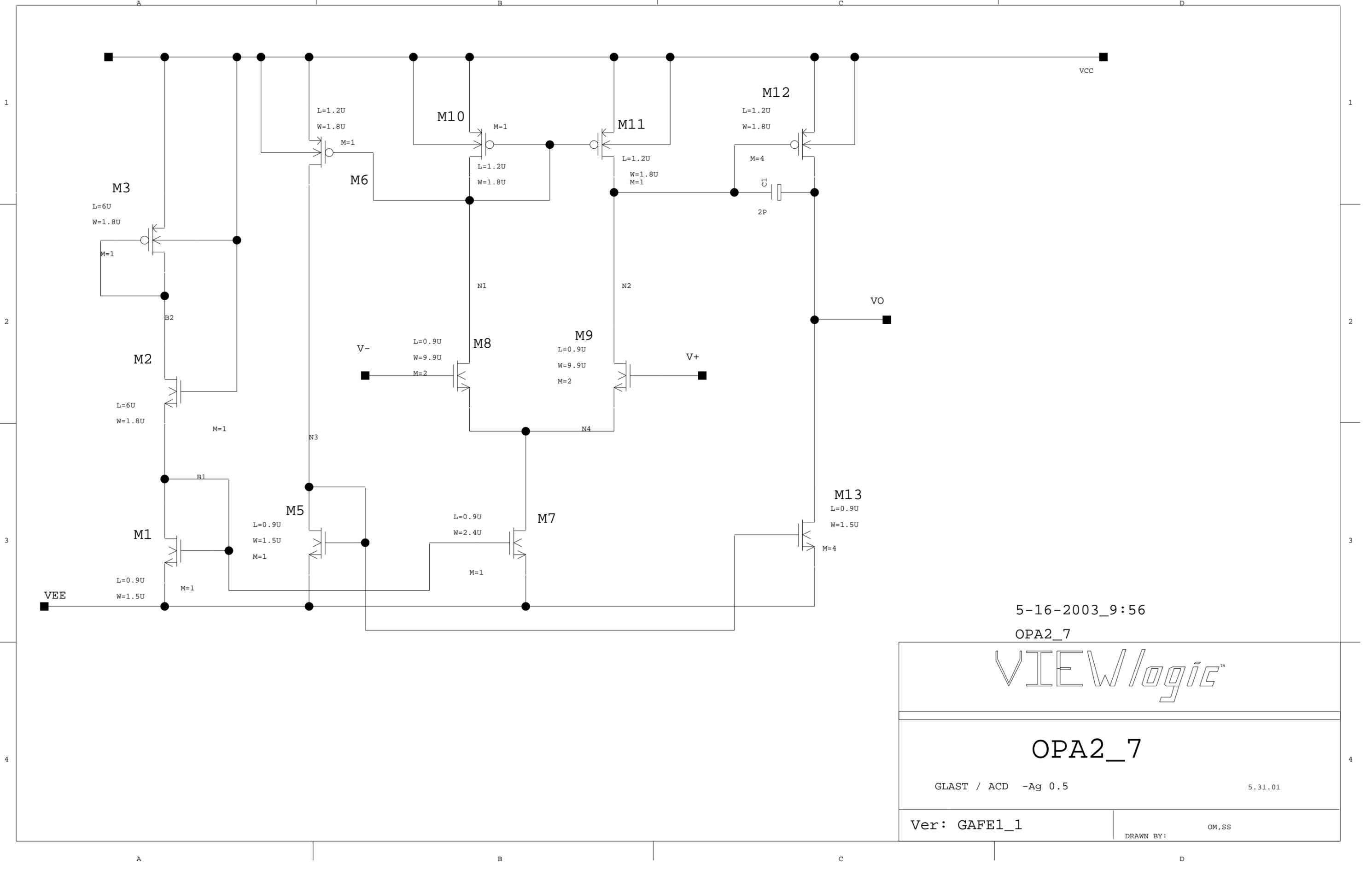
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GLAST / ACD -Ag 0.5

7.25.01

Ver: GAFE1_1

DRAWN BY: OM,SS



5-16-2003_9:56

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VIEWlogic™

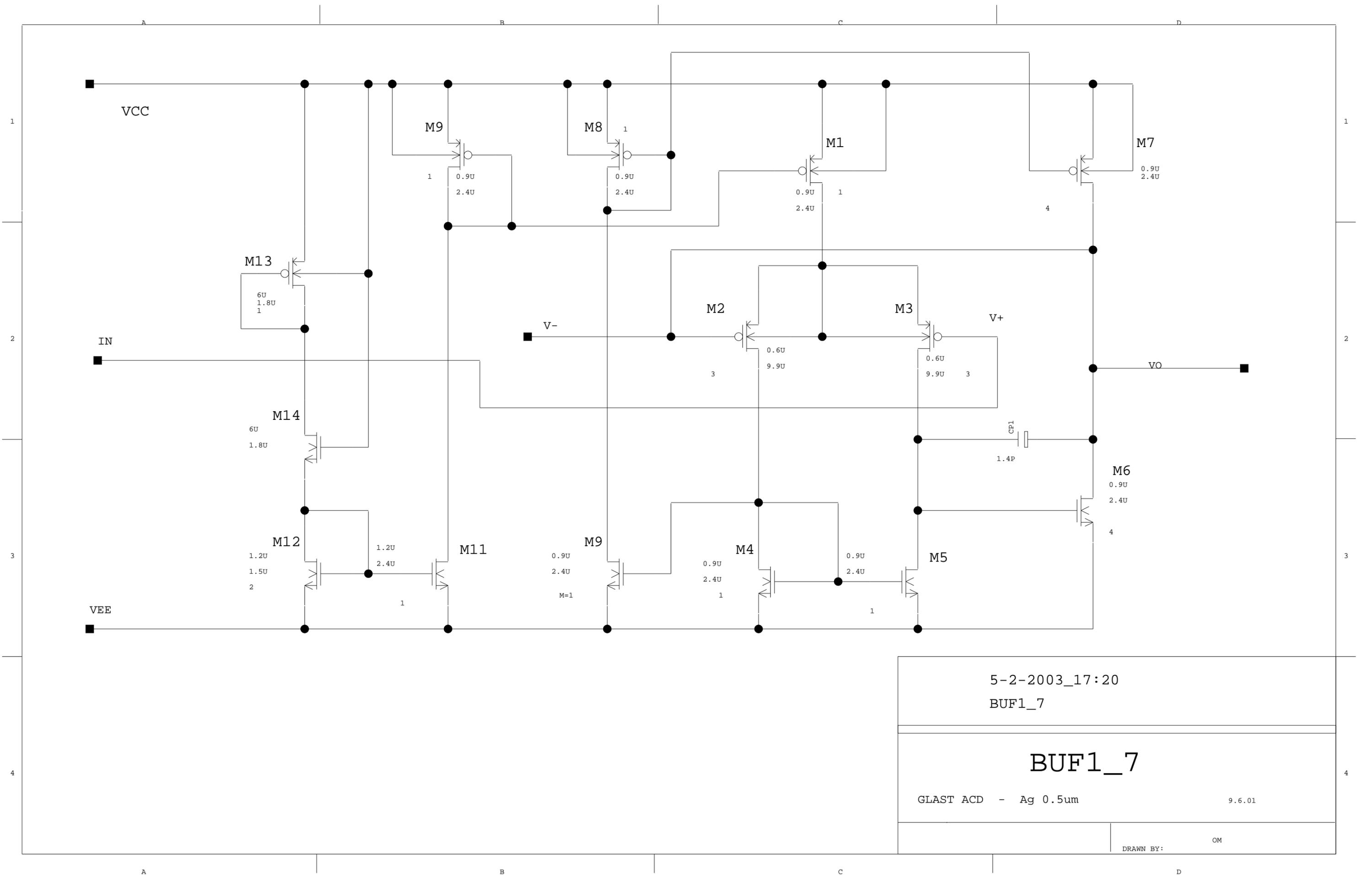
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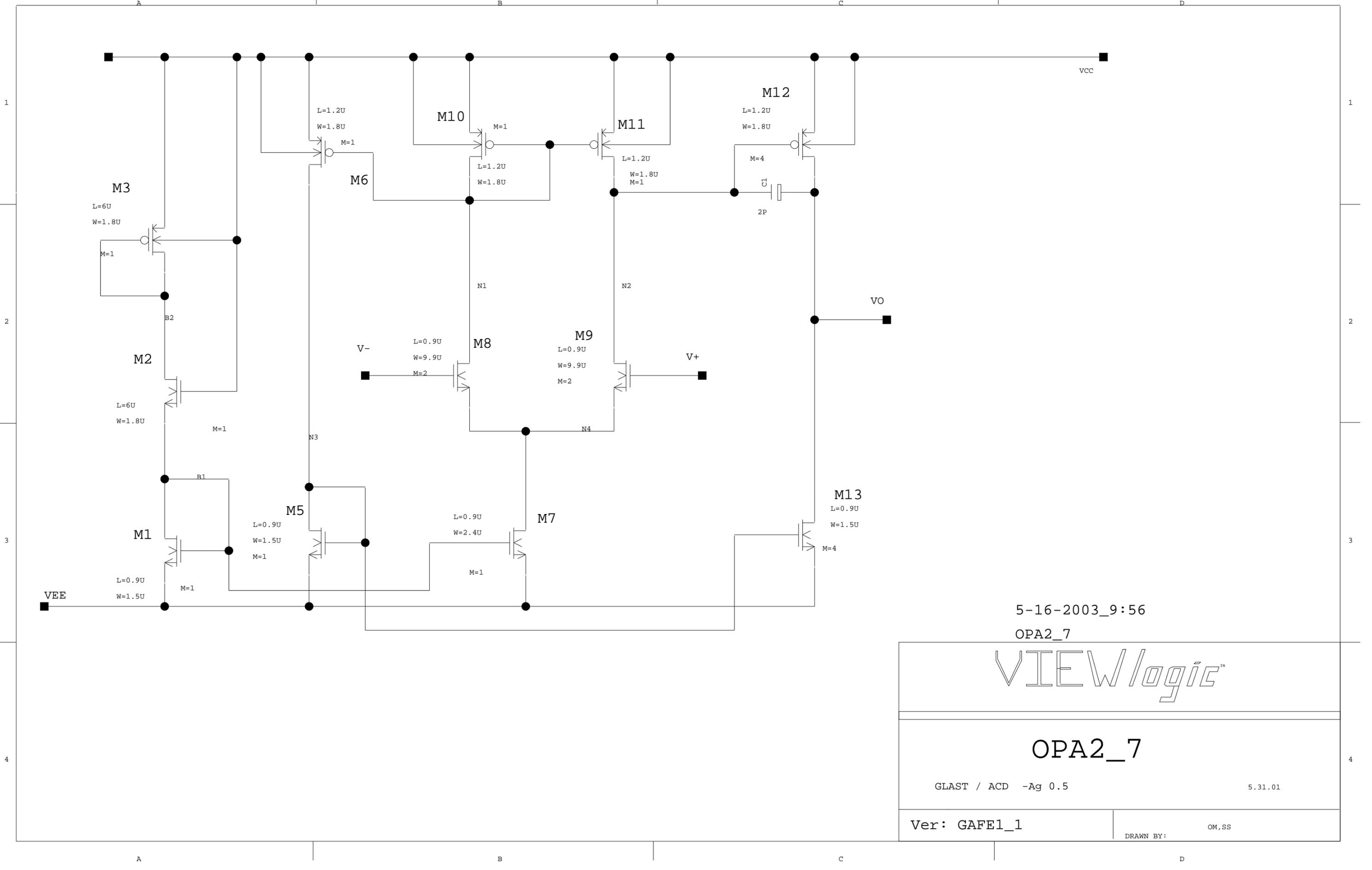
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 BUF1_7

BUF1_7

GLAST ACD - Ag 0.5um

9.6.01

DRAWN BY: OM



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VIEWlogic™

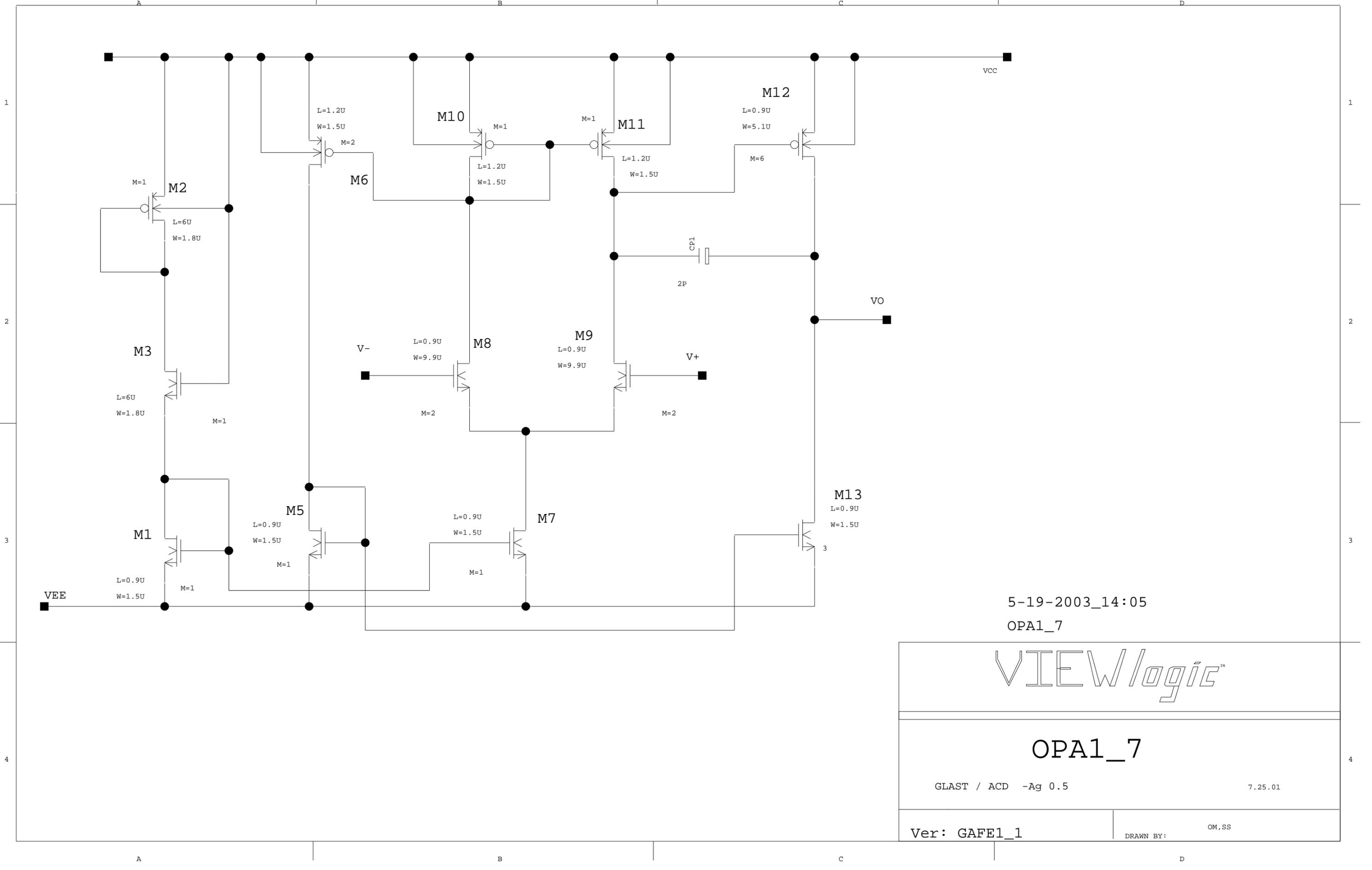
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Ver: GAFE1_1

DRAWN BY: OM,SS



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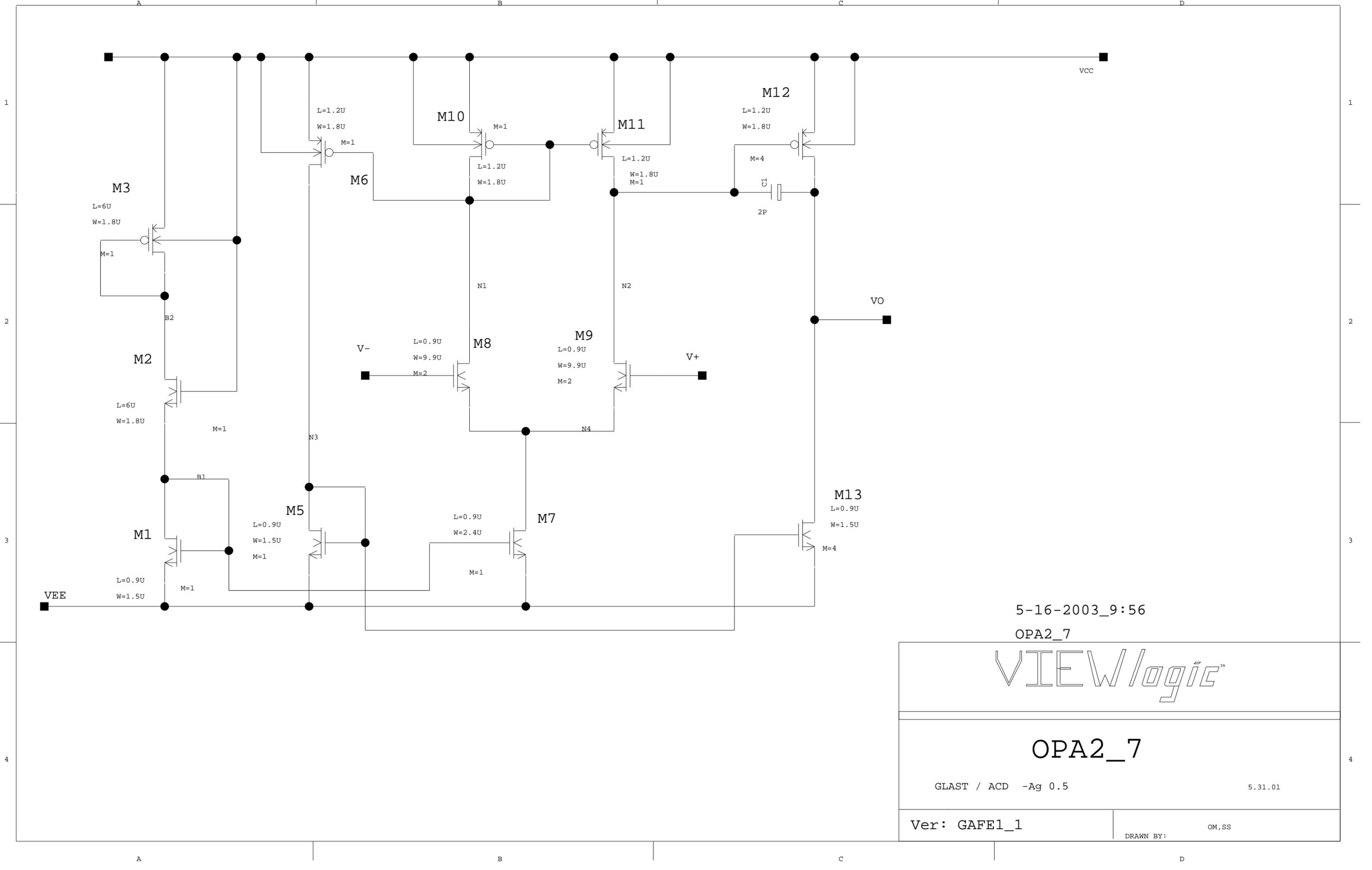
VIEWlogic™

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Ver: GAFE1_1

DRAWN BY: OM,SS



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VIEWlogic™

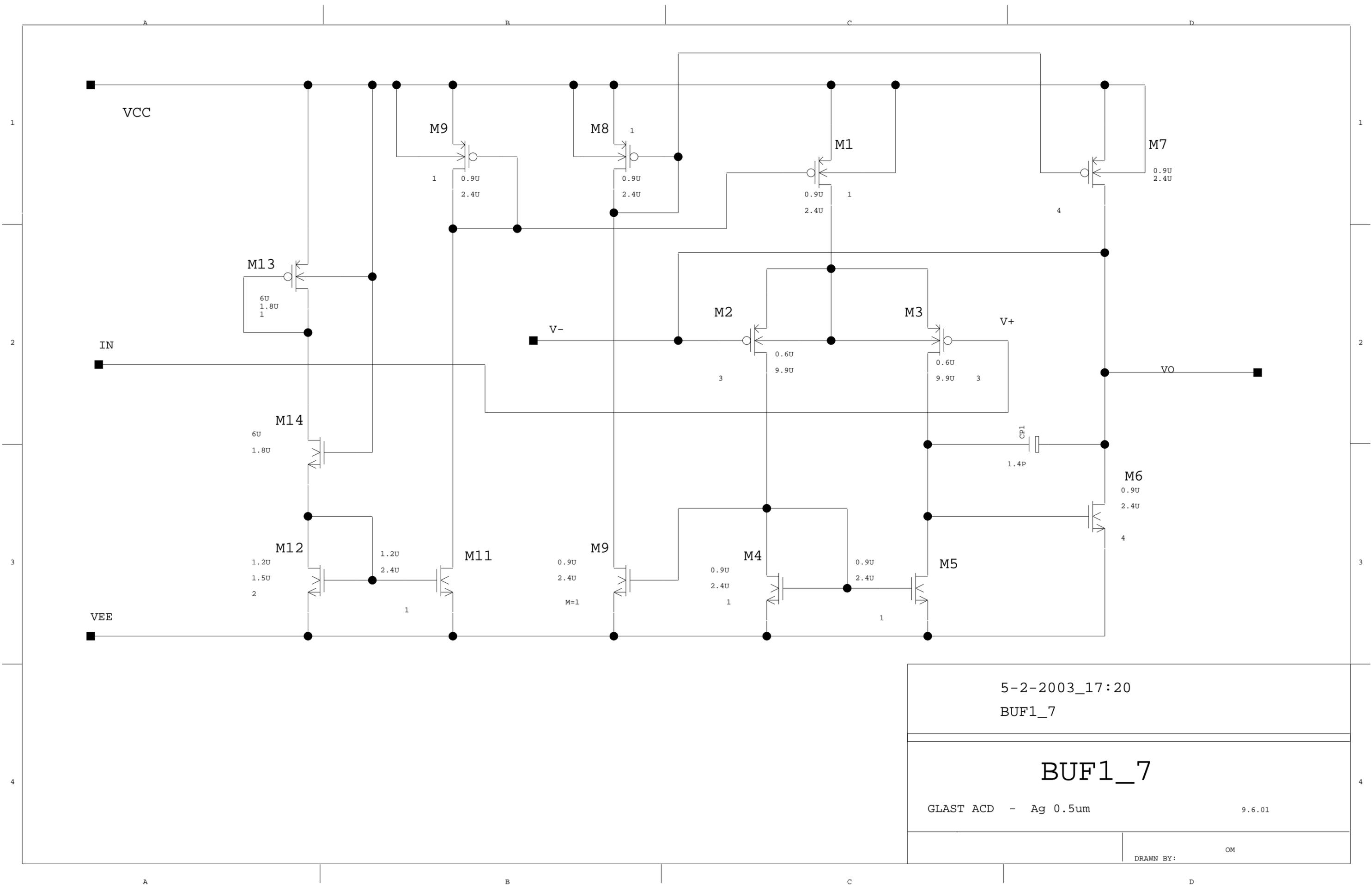
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Ver: GAFE1_1

DRAWN BY: OM,SS



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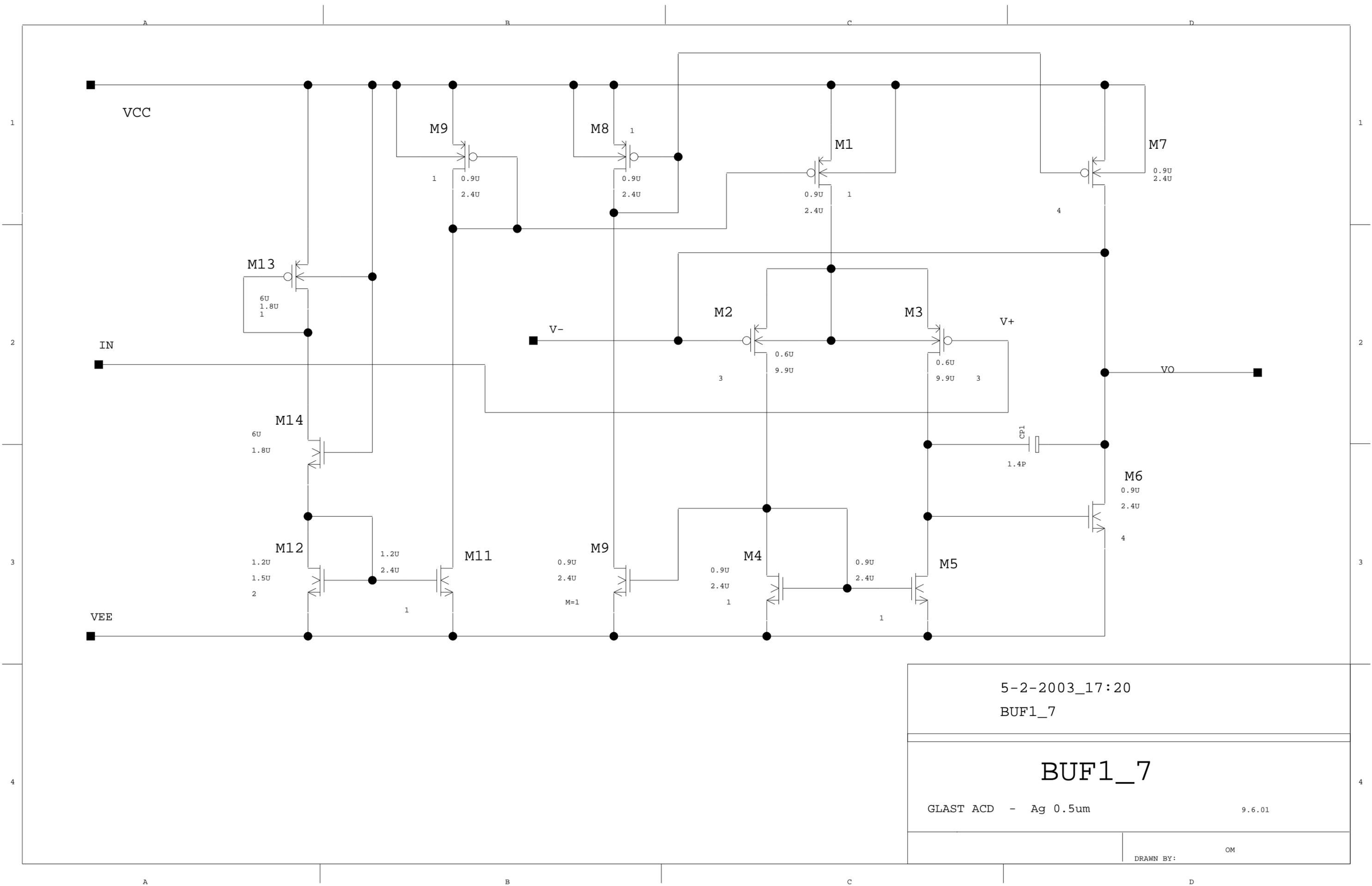
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BUF1_7

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9.6.01

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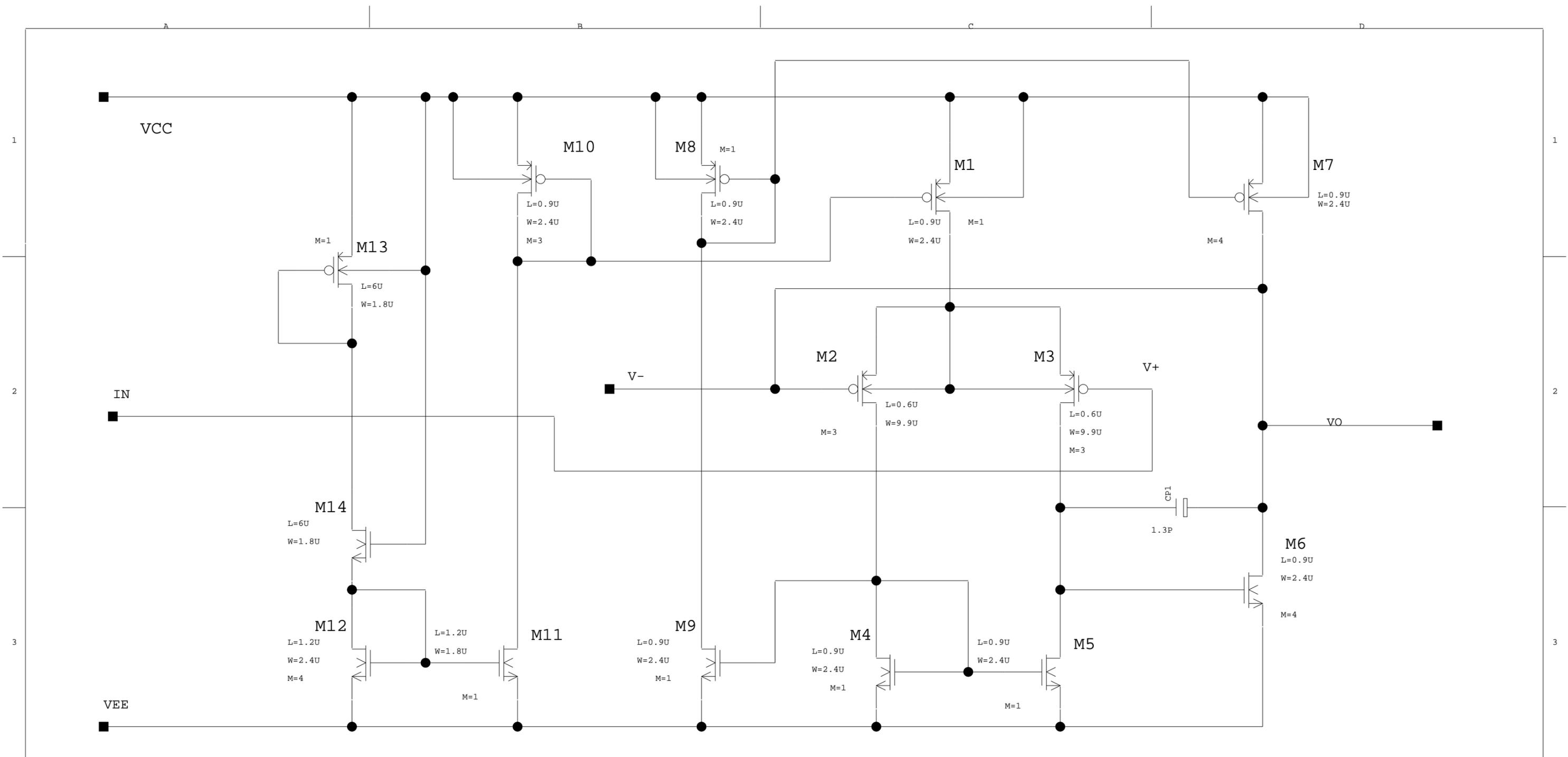
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DRAWN BY: OM



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BUFD1_7

BUFD1_7

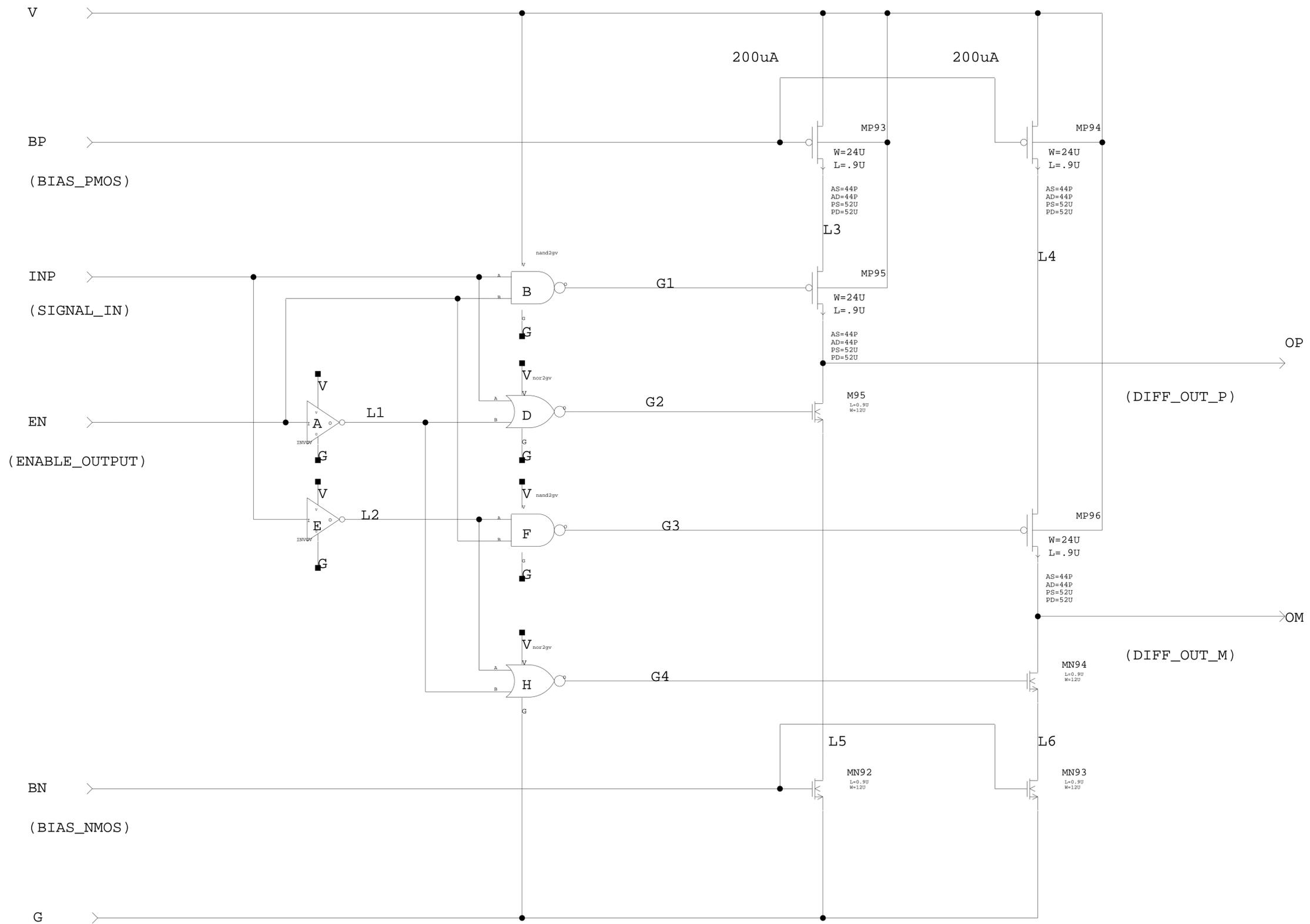
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Ver: GAFE1_1

DRAWN BY:

SATPAL SINGH

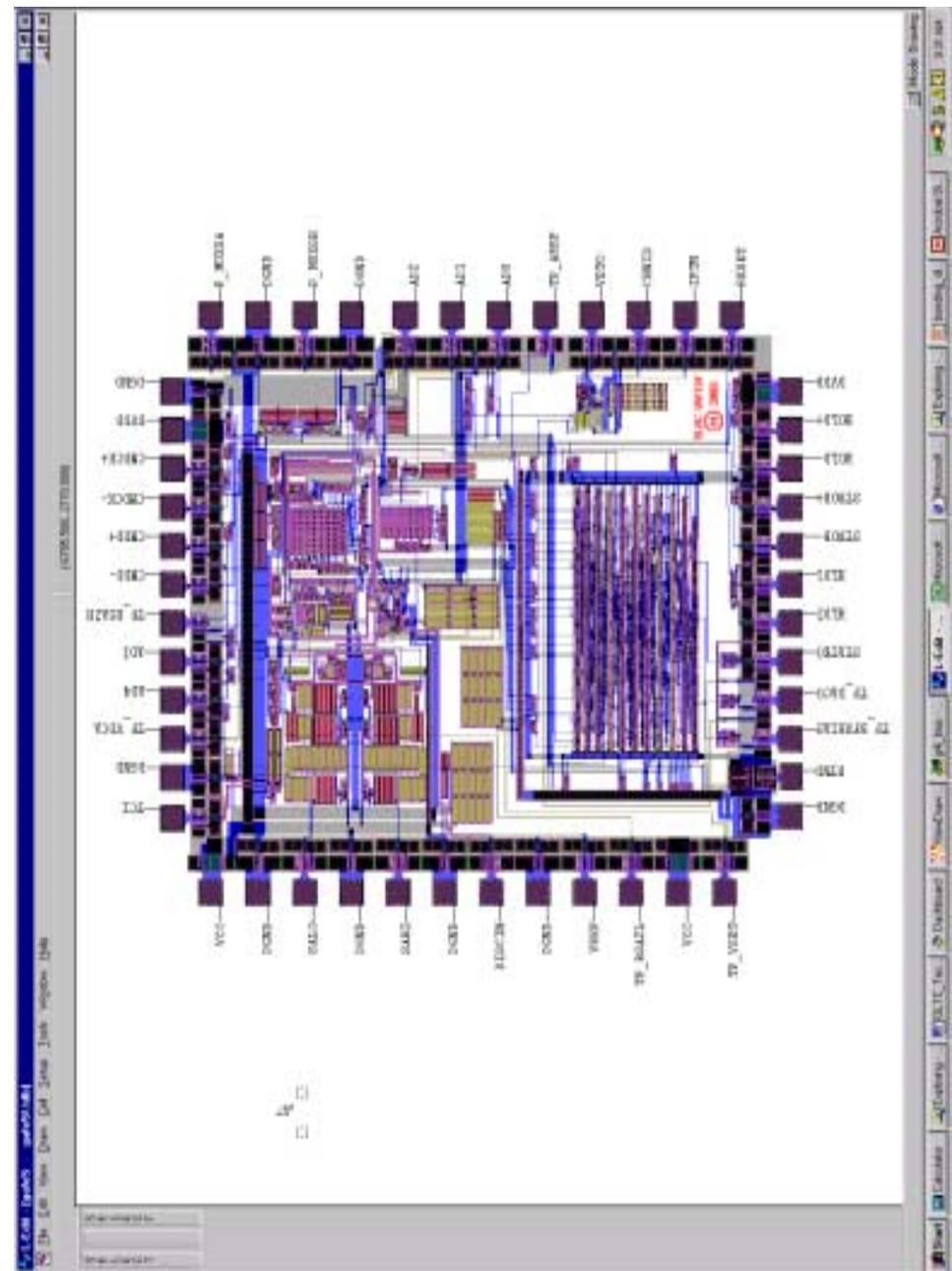


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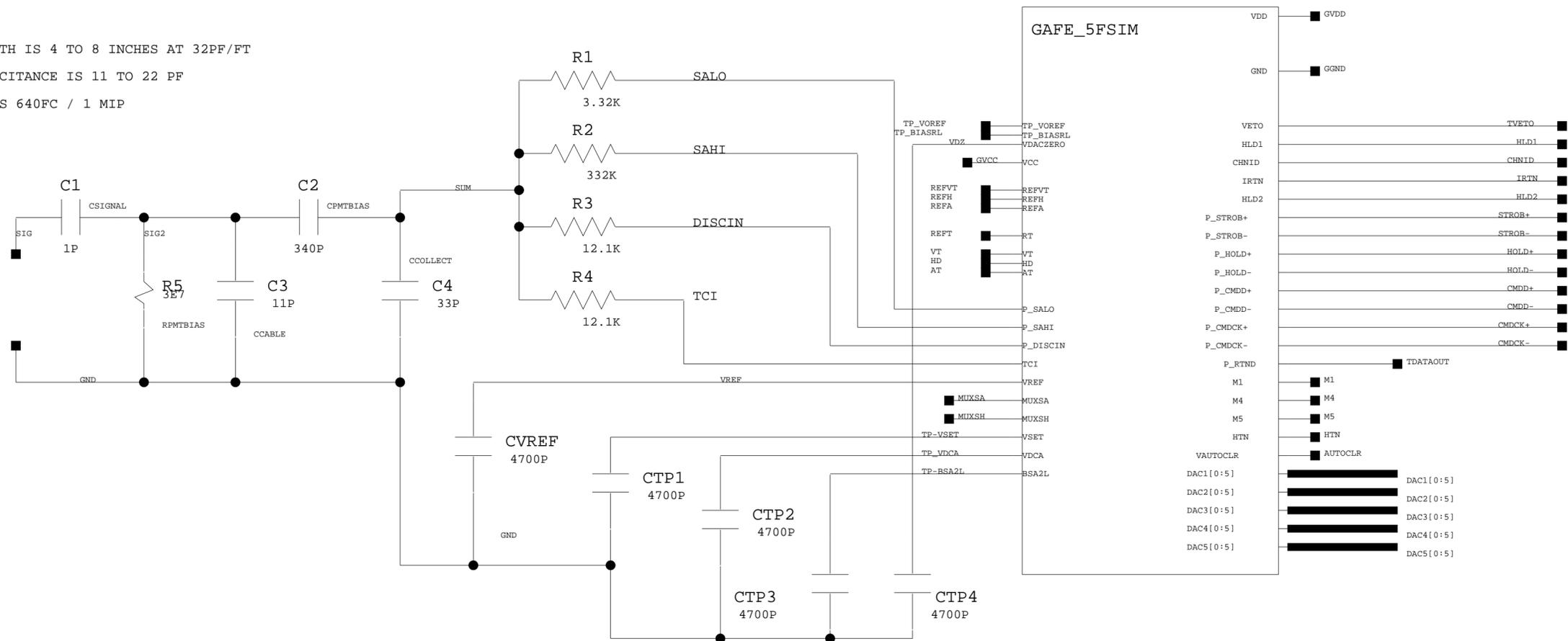
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DATE	APPROVALS	

GAFE5F PIN LIST
SLAC.COM.10DEC02

	Layout	Schematic	x	y
1	1 VCC	VCC		
2	2 GND	DGND		
3	3 SALO	P_SALO		
4	4 GND	DGND		
5	5 SAHI	P_SAHI		
6	6 GND	DGND		
7	7 DISCIN	P_DISCIN		
8	8 GND	DGND		
9	8 TP_VREF	TP_VREF		
10	9 TP_BSA2	TP_BSA2		
11	10 VCC	VCC		
12	11 TP_VSET	TP_VSET		
13	12 GND	DGND		
14	13 RTND	RTND		
15	14 TP_BFRBIAS	TP_BFRBIAS		
16	15 TP_DACZERO	TP_DACZERO		
17	16 HLD2	TP_STATE0		
18	17 HLD1	HLD1		
19	18 STROB-	P_STROB-		
20	19 STROB+	P_STROB+		
21	20 HOLD-	P_HOLD-		
22	21 HOLD+	P_HOLD+		
23	22 DVDD	DVDD		
24	23 RESET	RESET		
25	24 IRTN	IRTN		
26	25 CHNID	CHNID		
27	26 VETO	VETO		
28	27 TP_AREF	TP_AREF		
29	28 ADO	ADO		
30	29 AD1	AD1		
31	30 AD2	AD2		
32	31 MUXSH	MUXSH		
33	32 GND	DGND		
34	33 MUXSA	MUXSA		
35	34 GND	DGND		
36	35 DVDD	DVDD		
37	36 CMDCK+	P_CMDCK+		
38	37 CMDCK-	P_CMDCK-		
39	38 CMDD+	P_CMDD+		
40	39 CMDD-	P_CMDD-		
41	40 TP_BSA2H	TP_BSA2H		
42	41 AD3	AD3		
43	42 TP_VDCA	TP_VDCA		
44	43 GND	DGND		
45	44 TCI	TCI		
46	NC			
47	NC			
48	NC			



CABLE LENGTH IS 4 TO 8 INCHES AT 32PF/FT
 CABLE CAPACITANCE IS 11 TO 22 PF
 PMT GAIN IS 640FC / 1 MIP



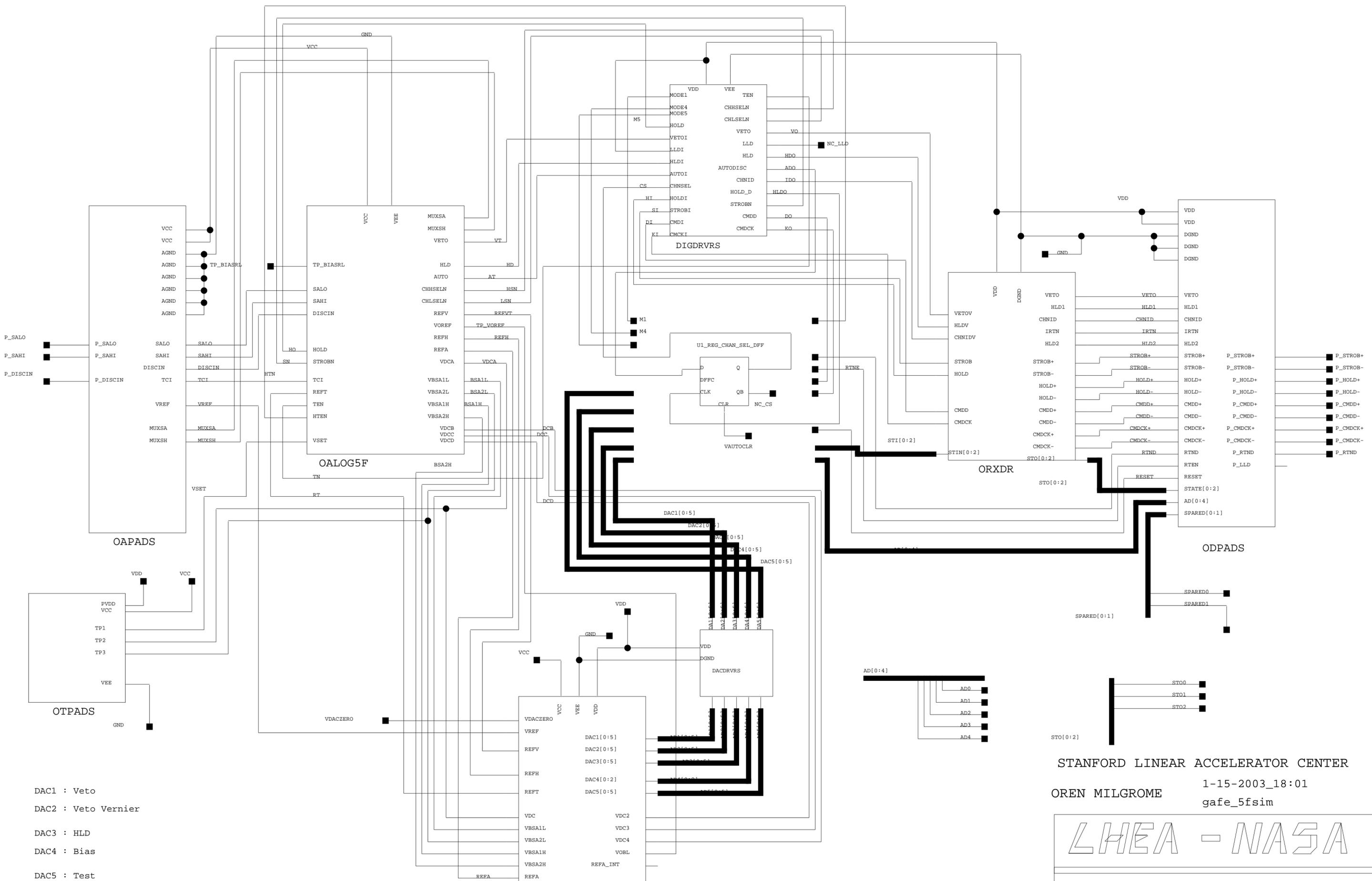
STANFORD LINEAR ACCELERATOR CENTER

1-16-2003_2:55

gafe5f_testbench



DRAWN BY:



DAC1 : Veto
 DAC2 : Veto Vernier
 DAC3 : HLD
 DAC4 : Bias
 DAC5 : Test

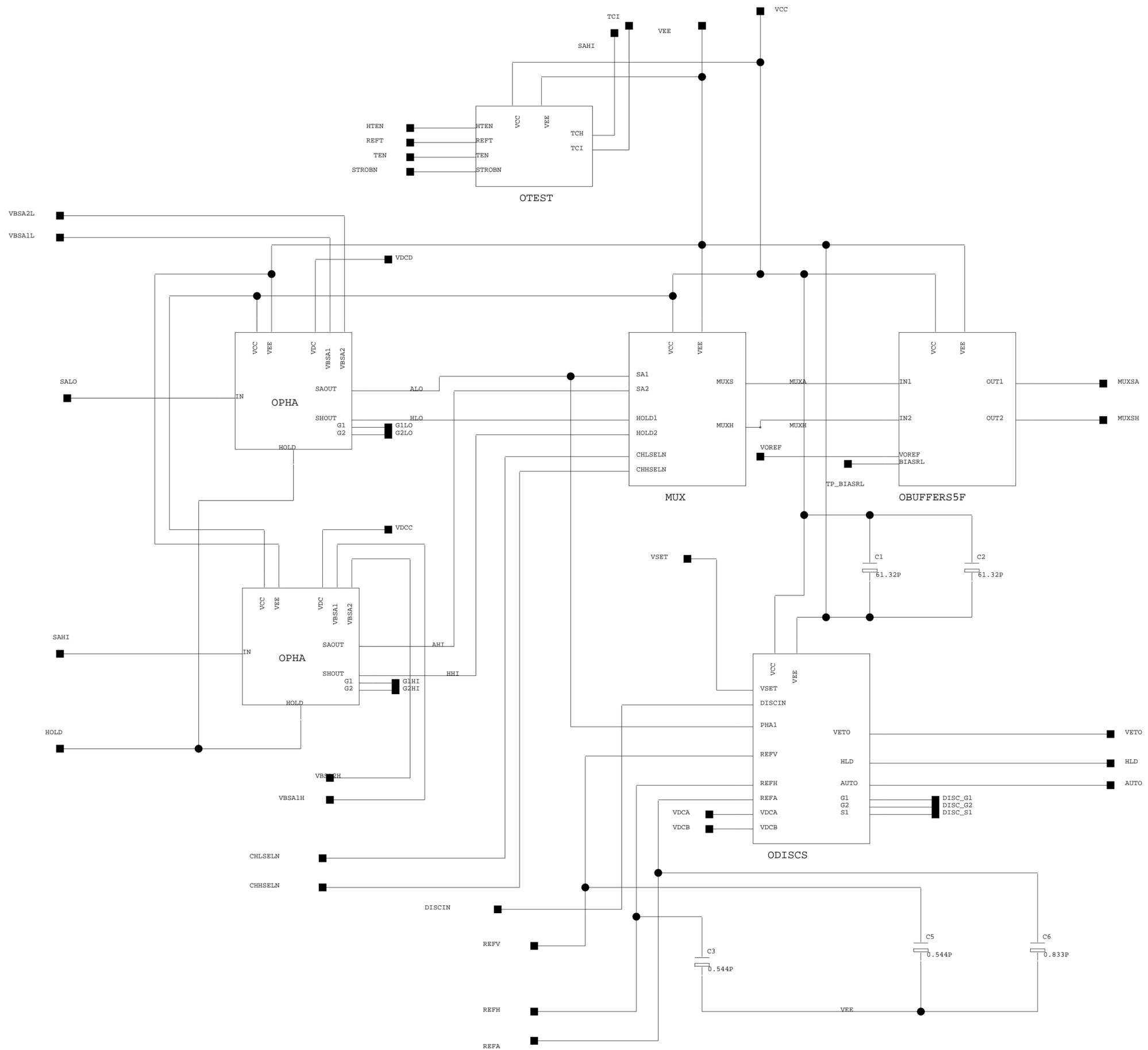
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 MODE1 : LOW RANGE CAL ENABLE
 MODE4 : VETO DISCRIMINATOR ENABLE
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STANFORD LINEAR ACCELERATOR CENTER
 OREN MILGROME 1-15-2003_18:01
 gafe_5fsim

LHEA - NASA

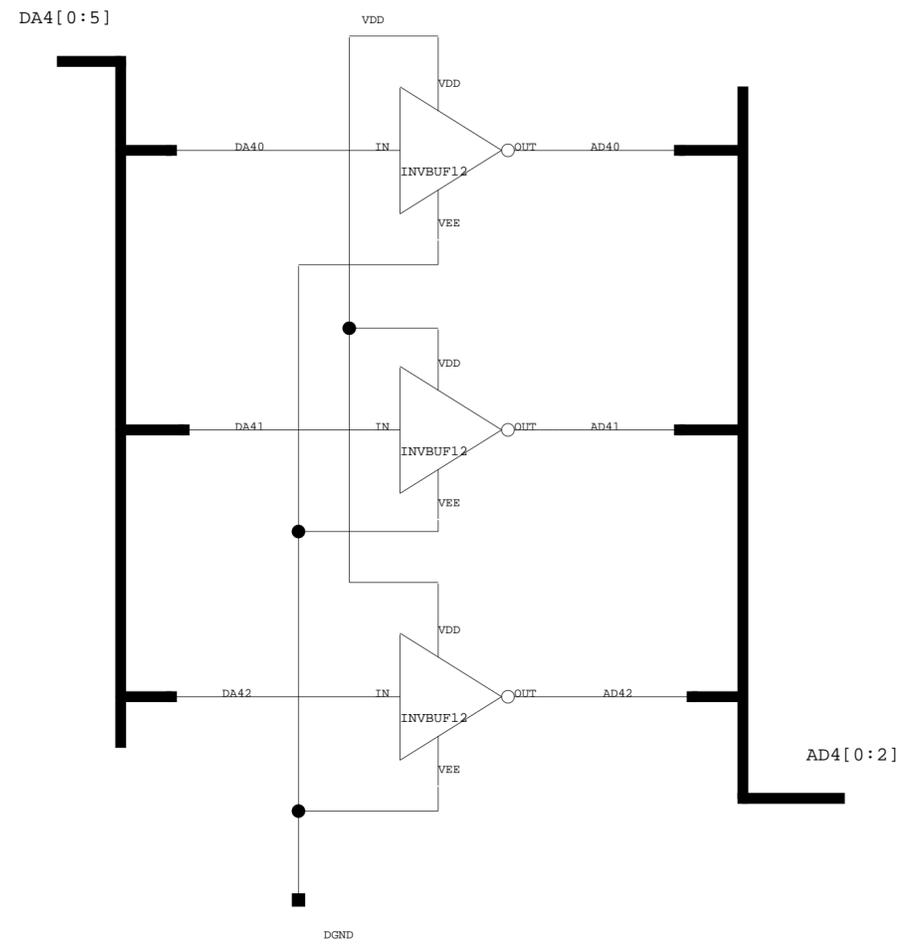
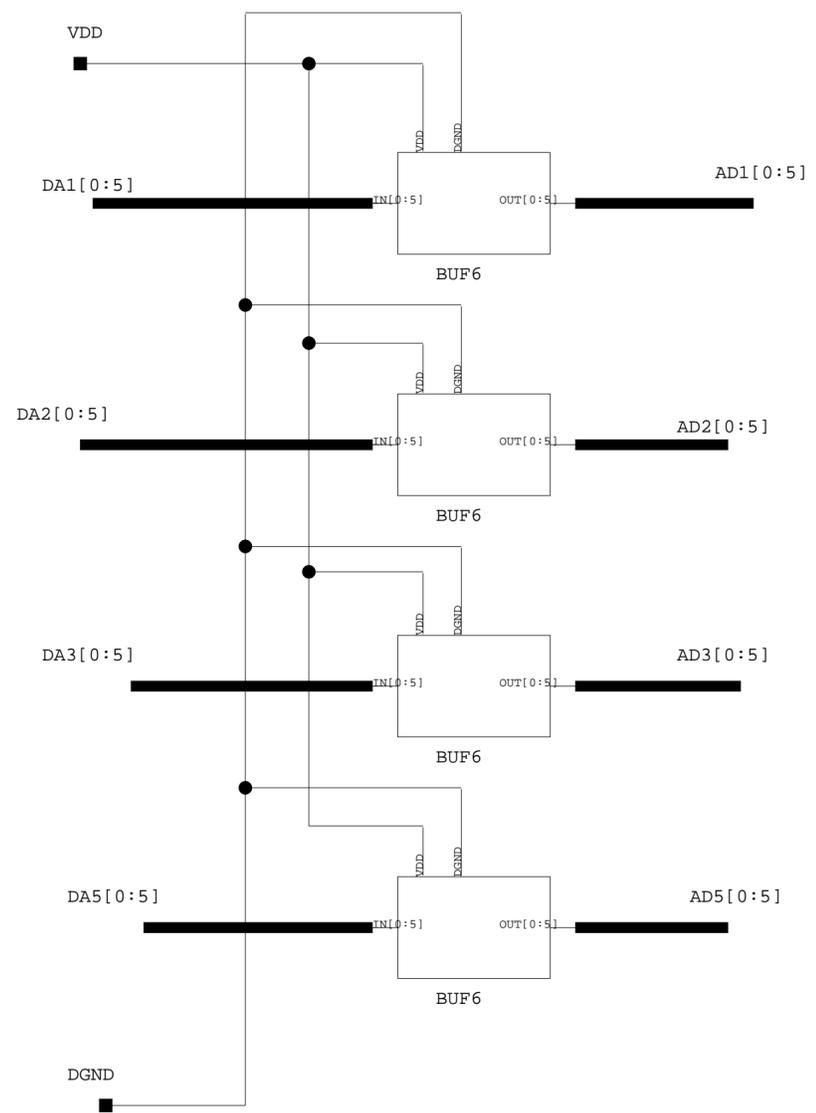
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ver: GAFE4 Satpal Singh, Oren Milgrome
DRAWN BY:



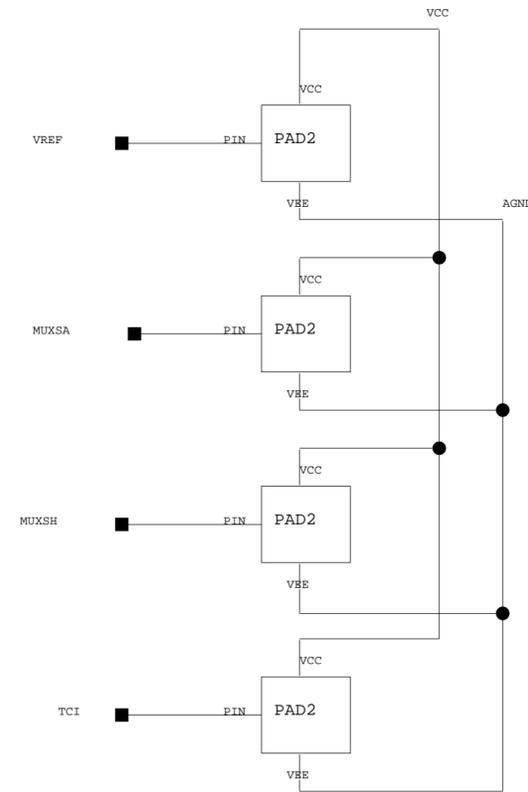
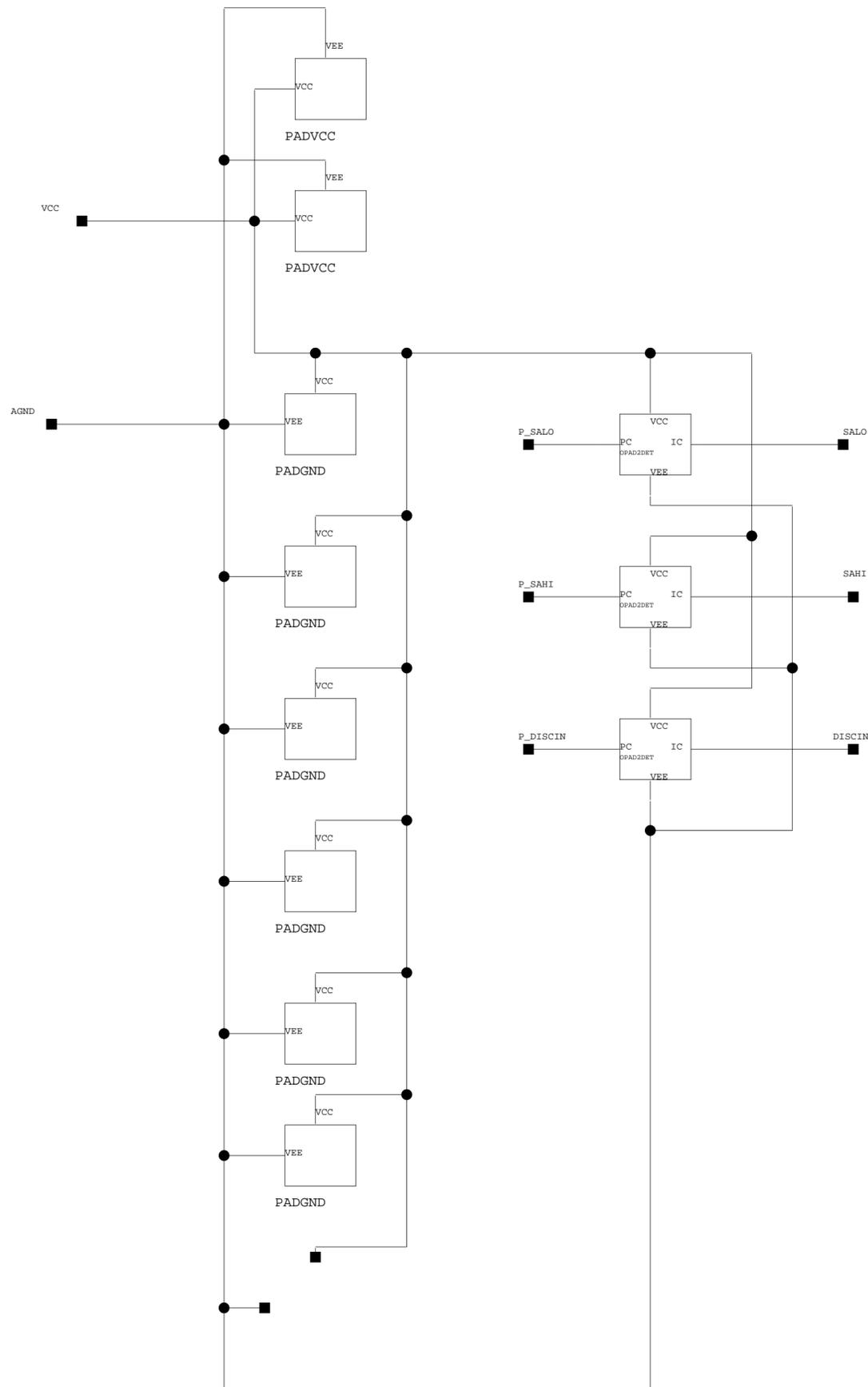
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Proj: GLAST ACD	
ver: GAFB1_1	DRAWN BY: Satpal Singh



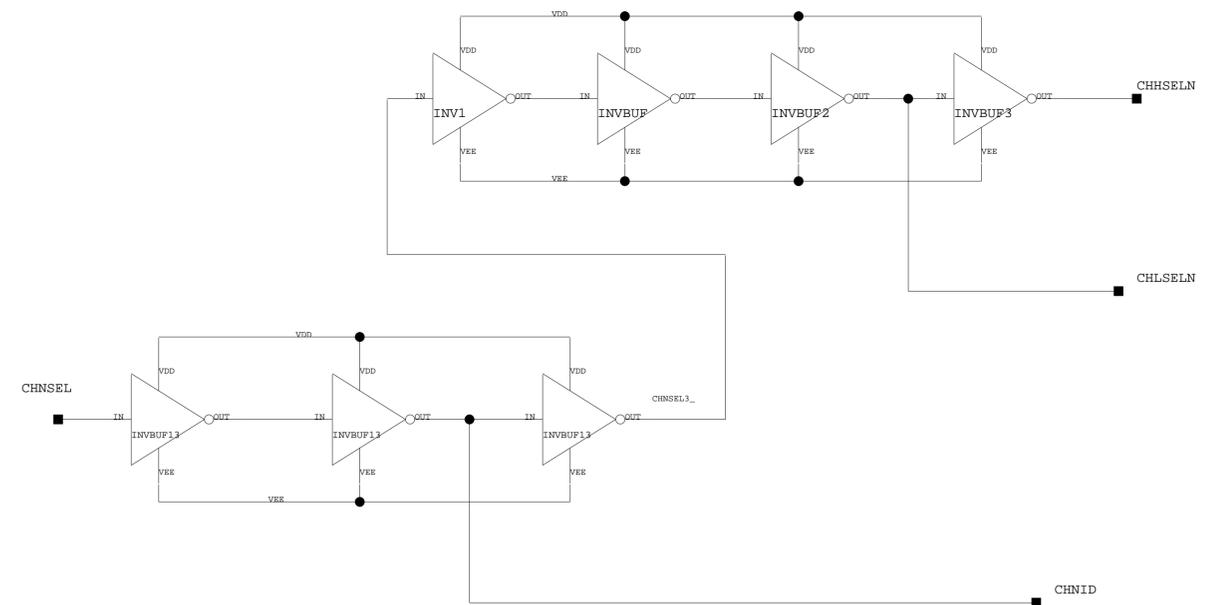
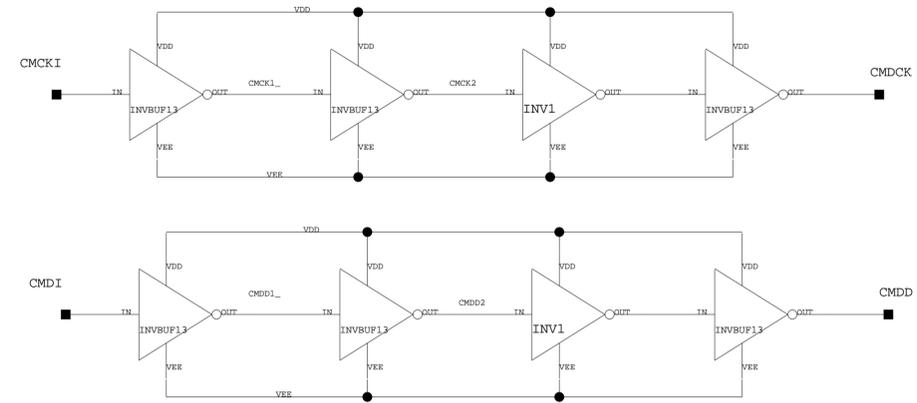
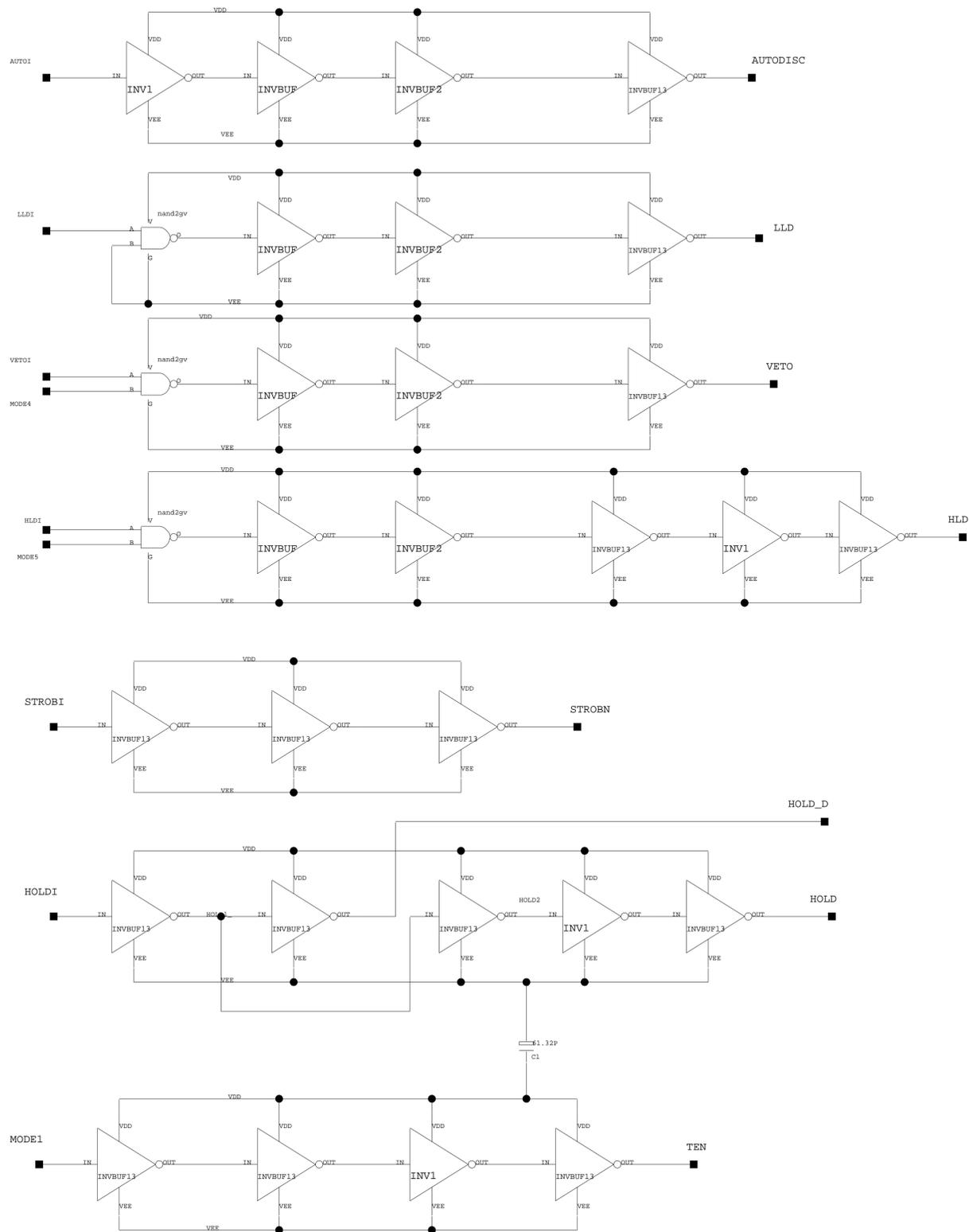
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DACDRVRS	
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ver: GAFE1_1	DRAWN BY: Satpal Singh



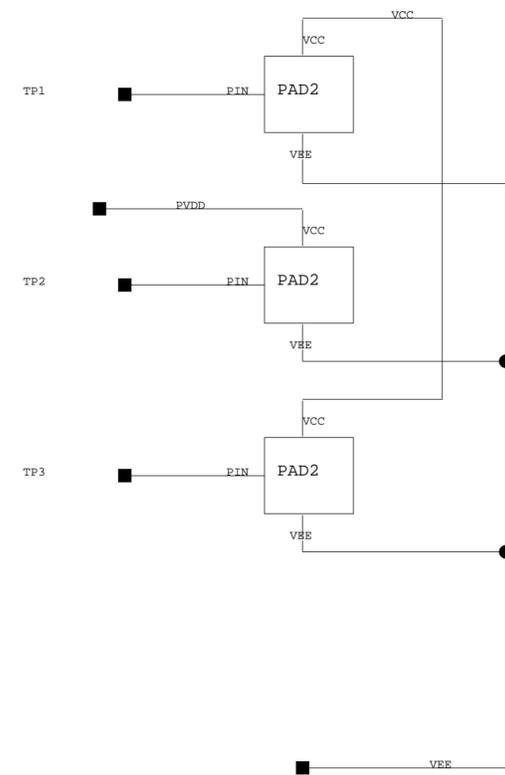
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9-17-2002_14:54
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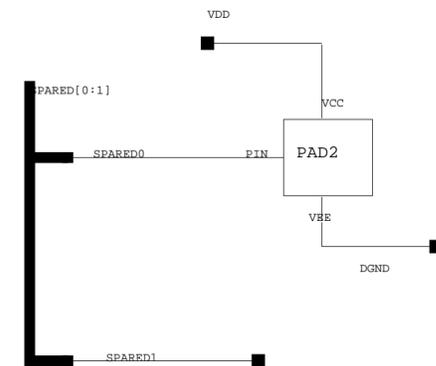
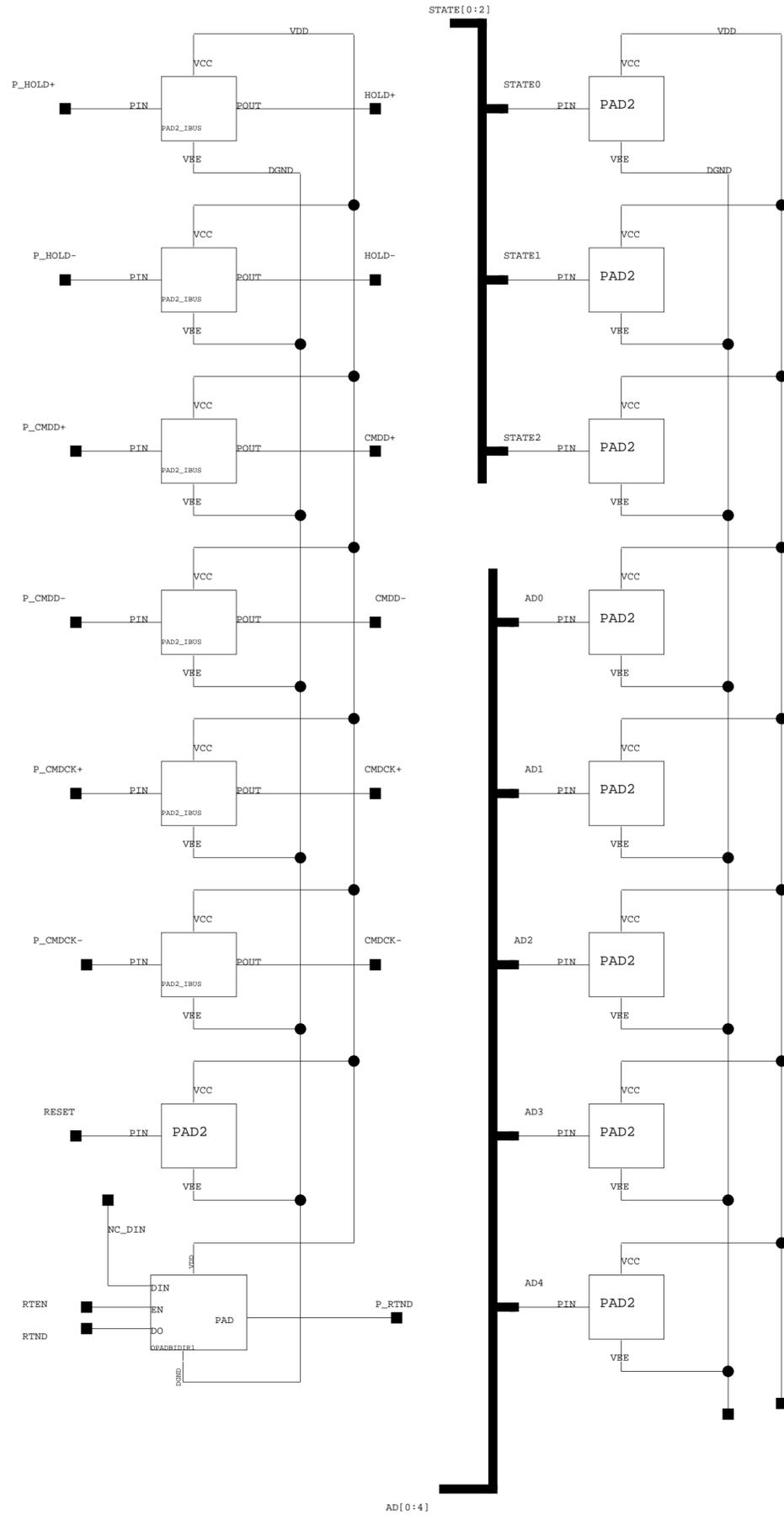
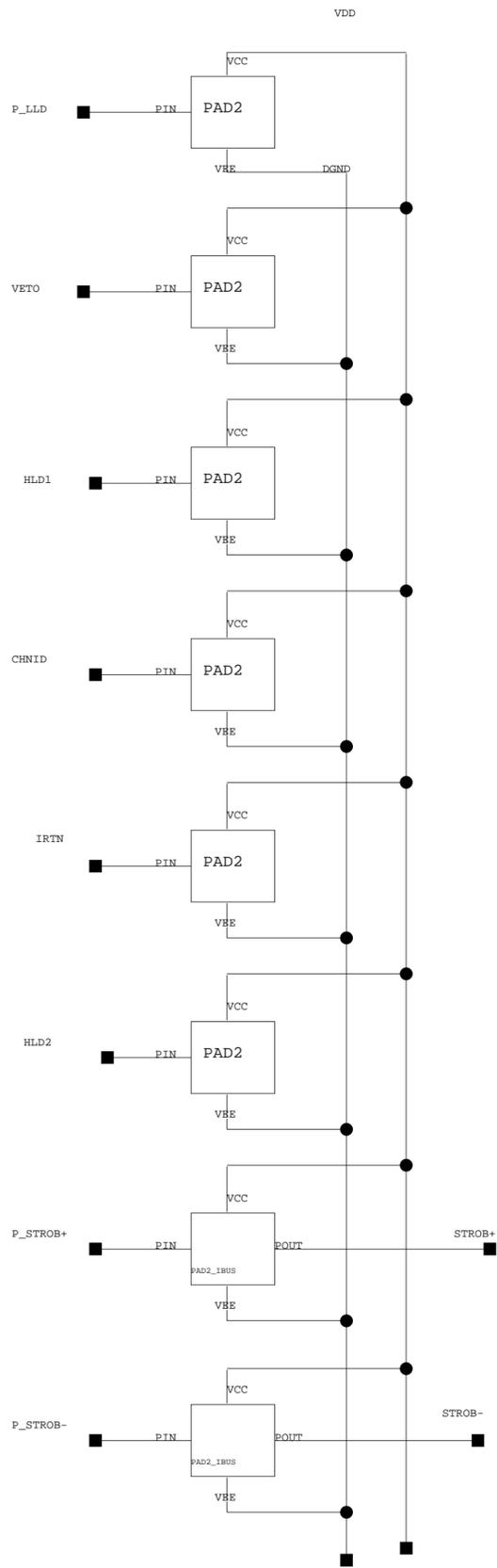
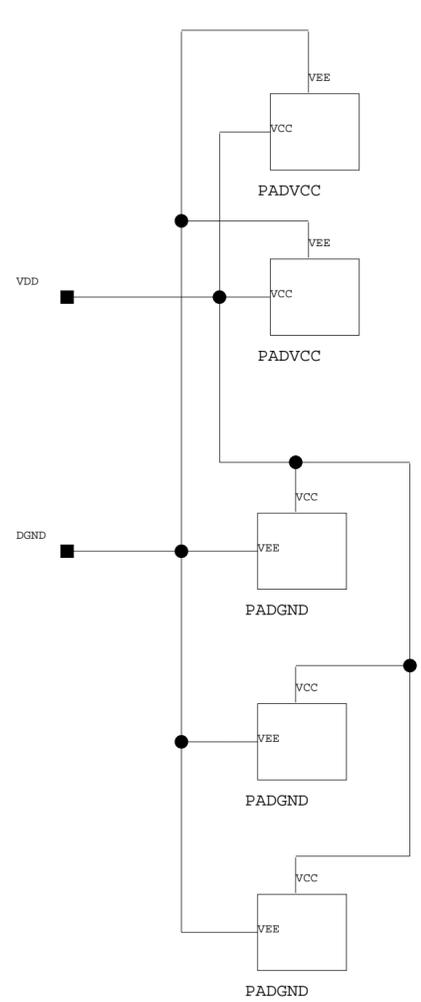
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11-15-2002_5:59

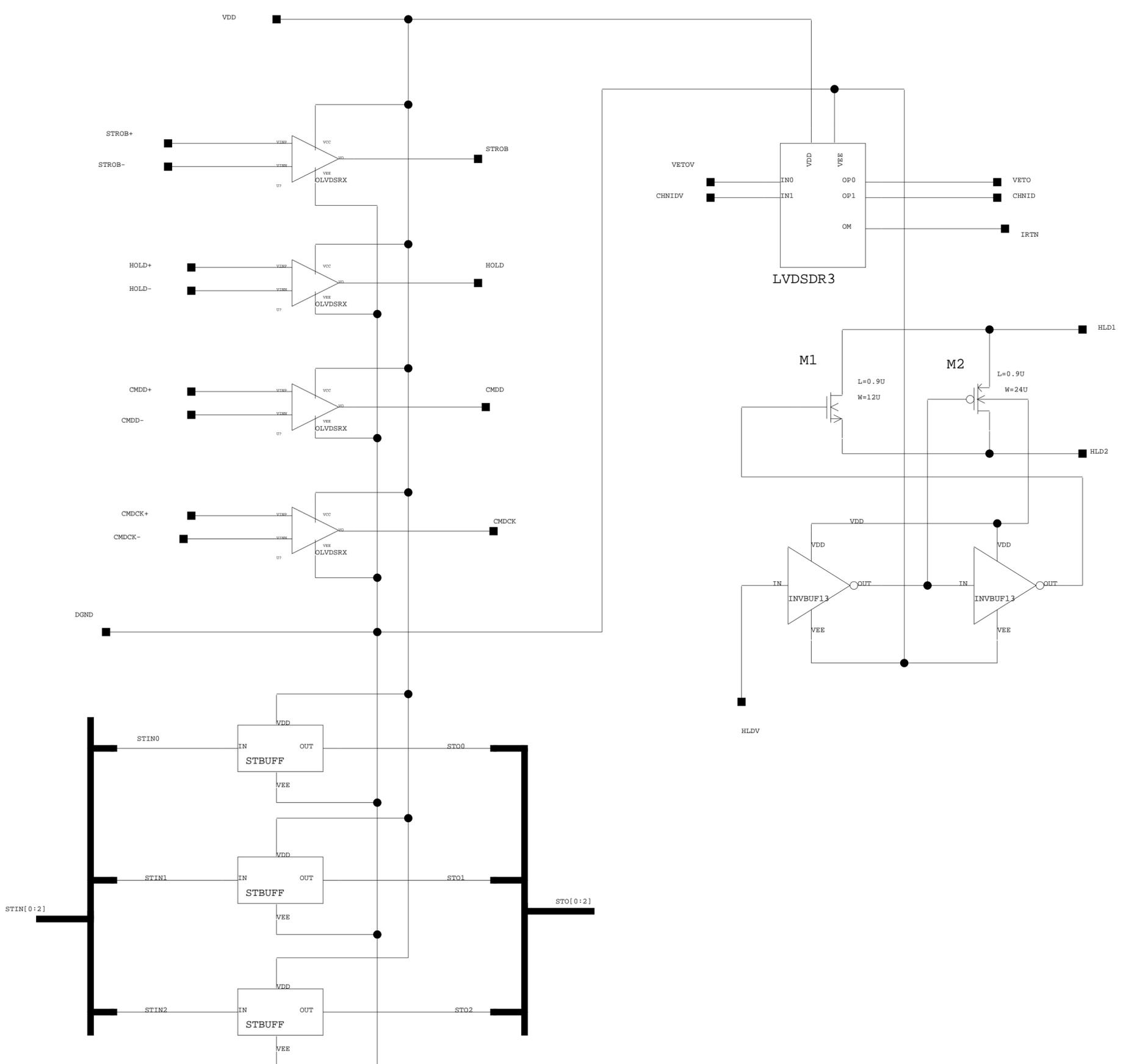
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11-15-2002_6:28
ODPADS

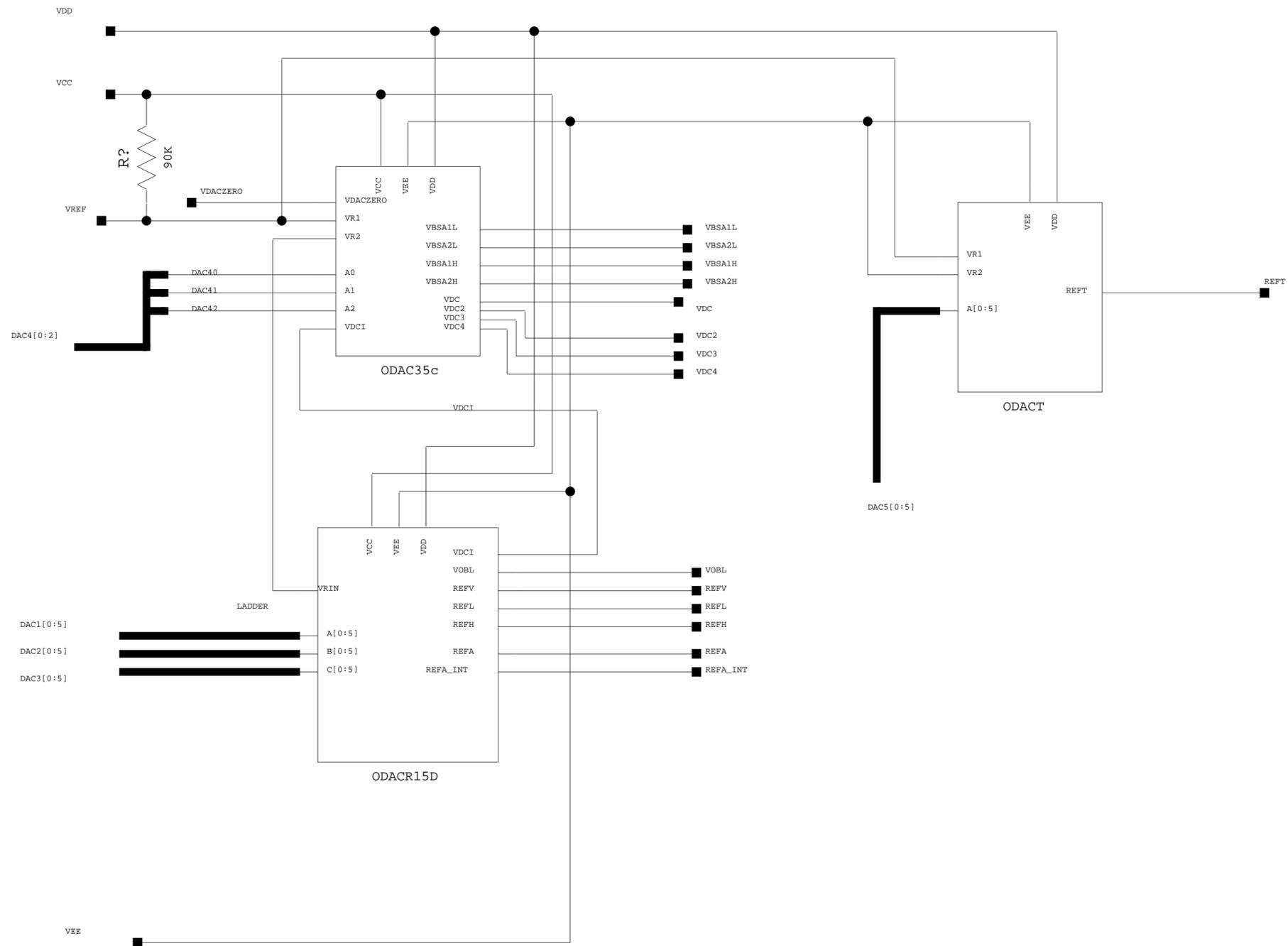
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10-24-2002_16:20

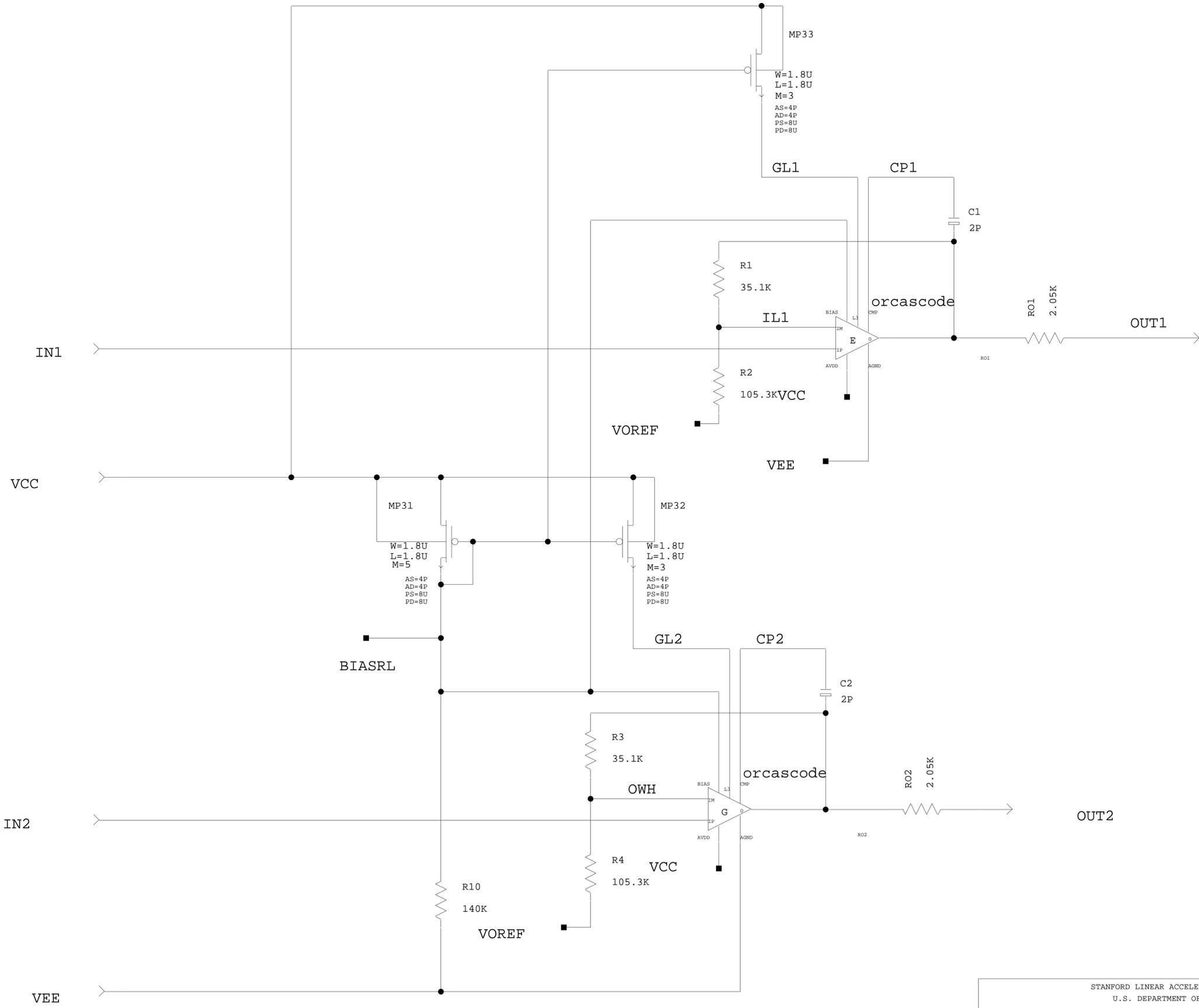
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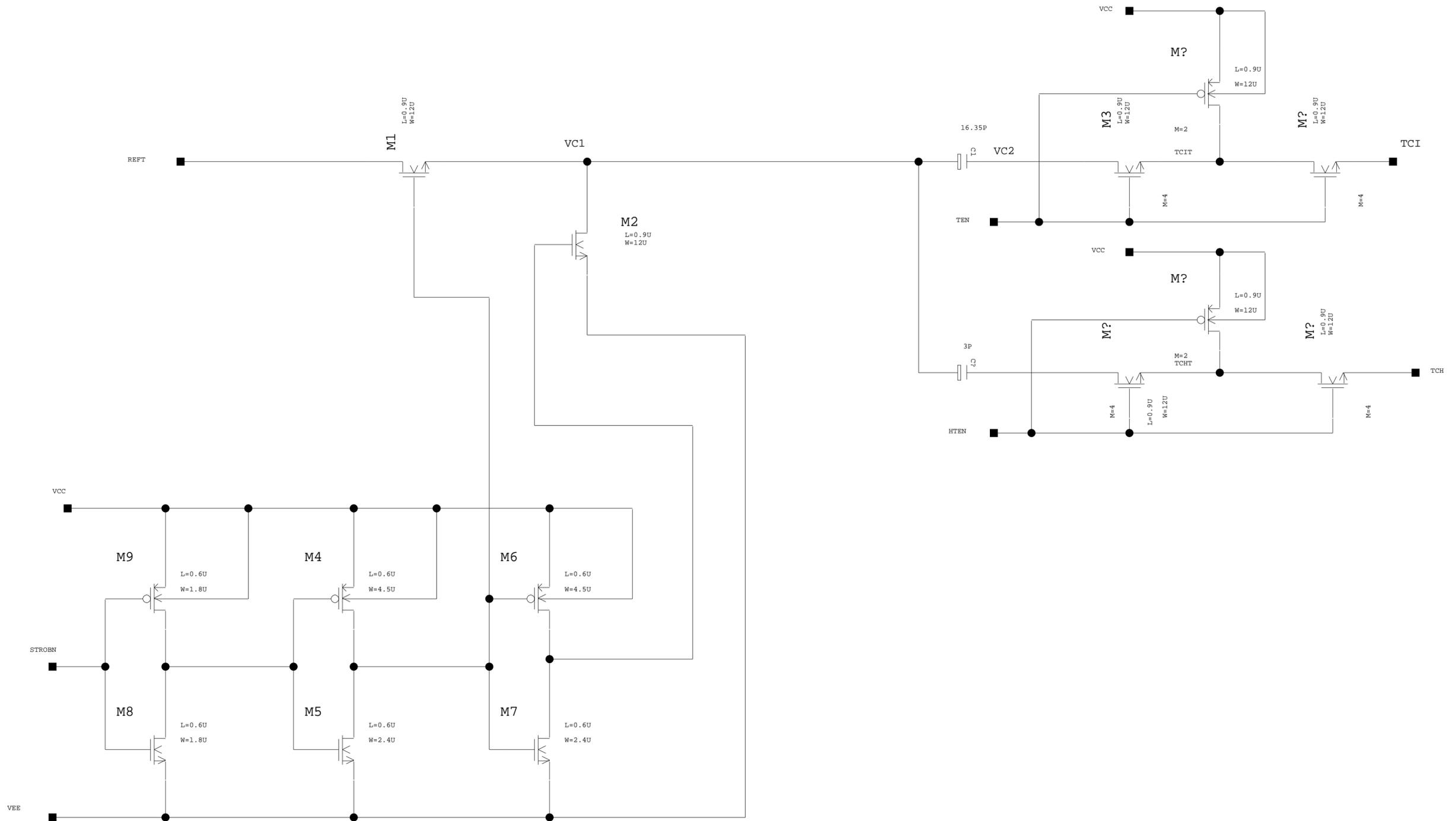
1-3-2003_5:08
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LHEA - NASA	
DACs	3.6.02
Proj: GLAST ACD	
ver: GAFE1_1	DRAWN BY: Satpal Singh



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DATE	DATE	APPROVALS

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10-31-2002_12:44

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LHEA - NASA

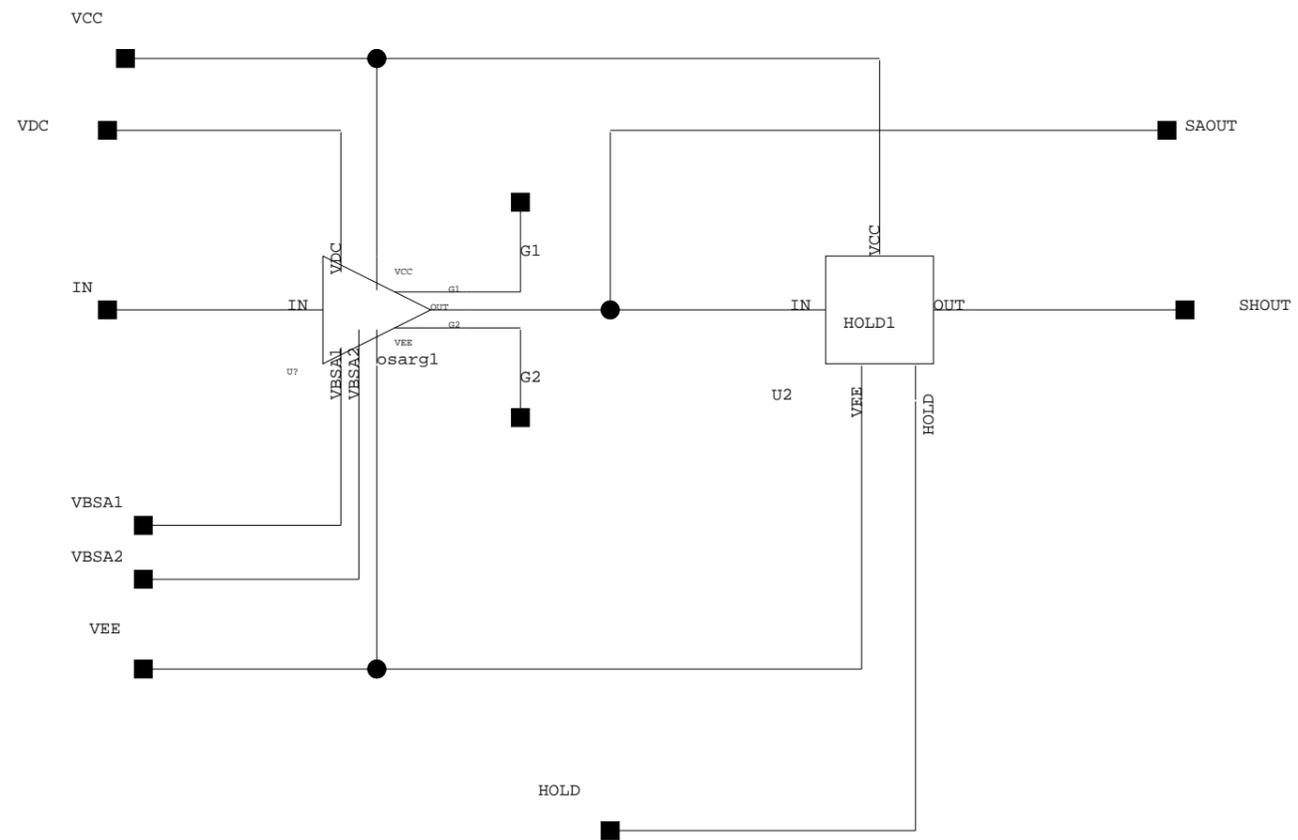
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GLAST ACD

10.11.01

Ver: GAFE1_1

DRAWN BY: SATPAL SINGH



11-13-2002_12:19

OPHA

LHEA - NASA

PHA

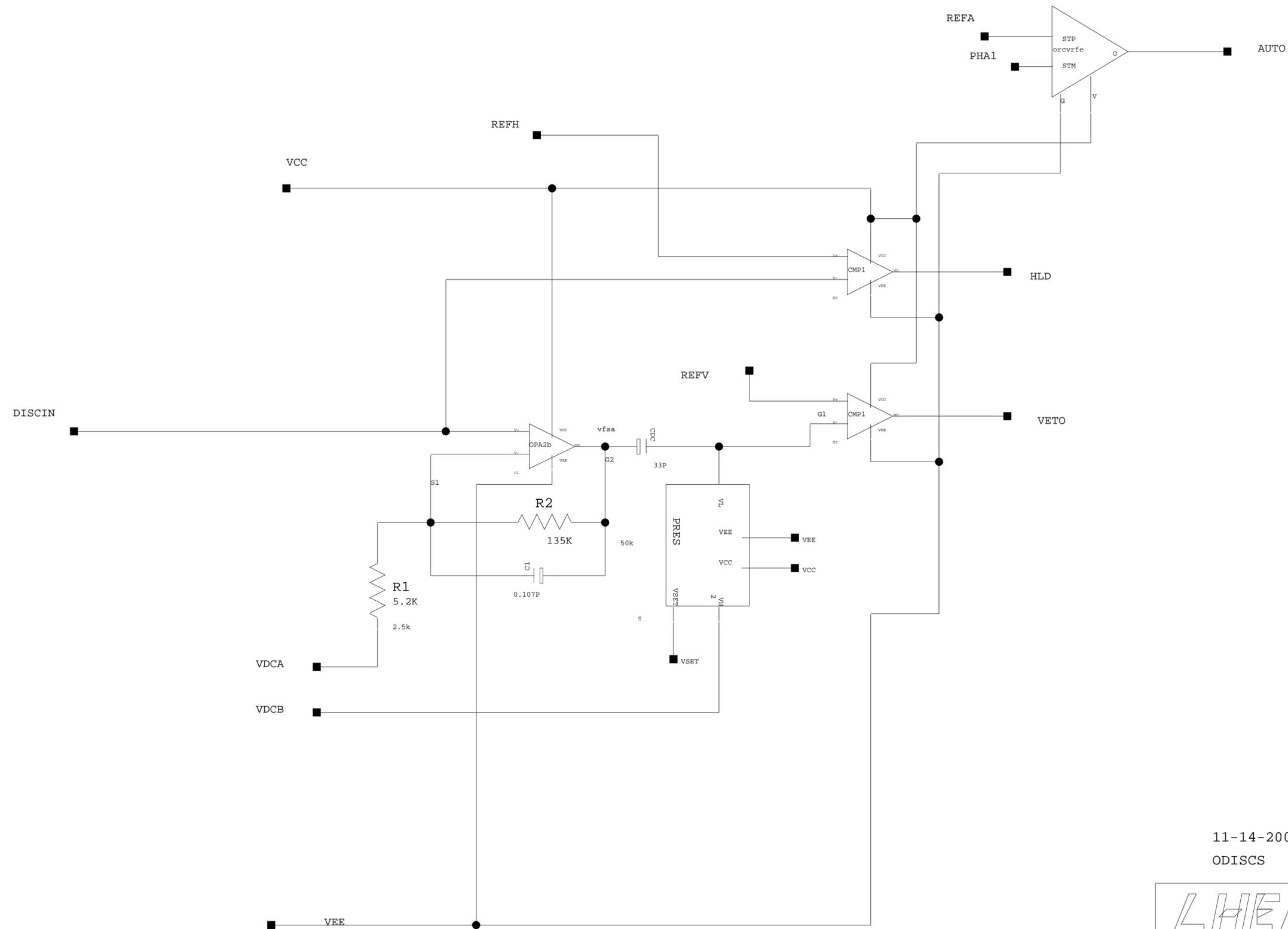
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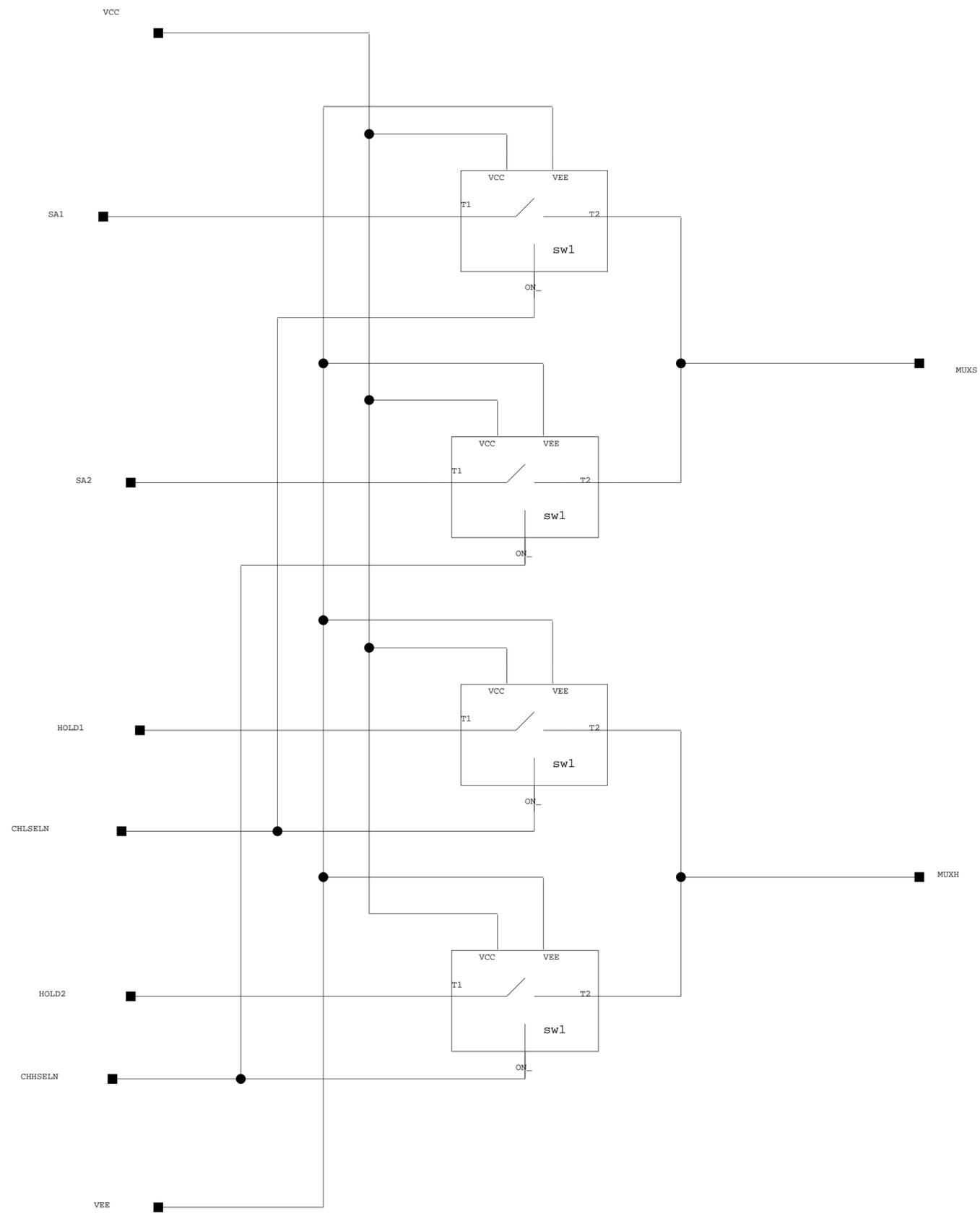
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Satpal Singh



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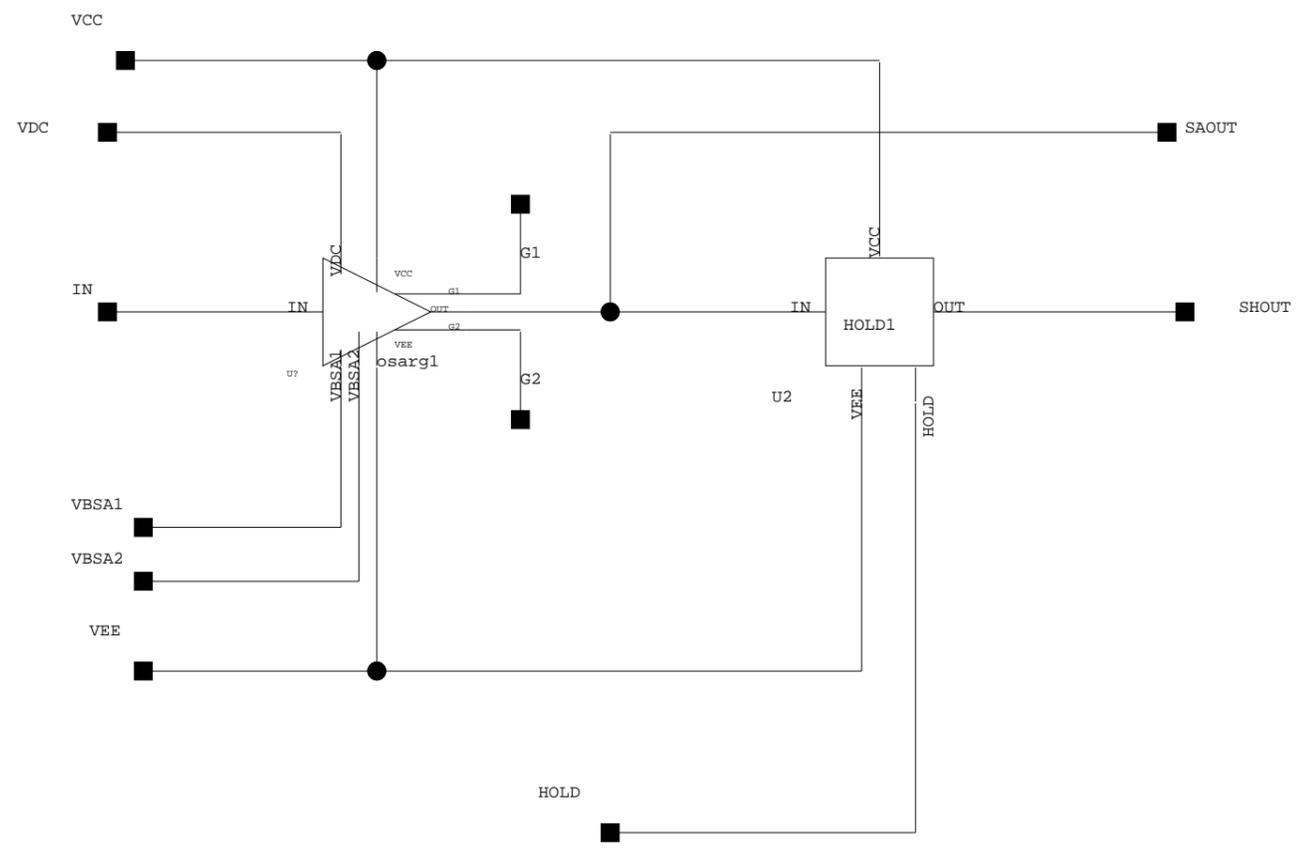
LHEA - NASA	
ODISCS	3.6.02
Proj: GLAST ACD	
ver: GAF1_1	S. SINGH/ O. MILGROME DRAWN BY:



5-9-2002_15:13

mux

<h1>LHEA - NASA</h1>	
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11-13-2002_12:19

OPHA

LHEA - NASA

PHA

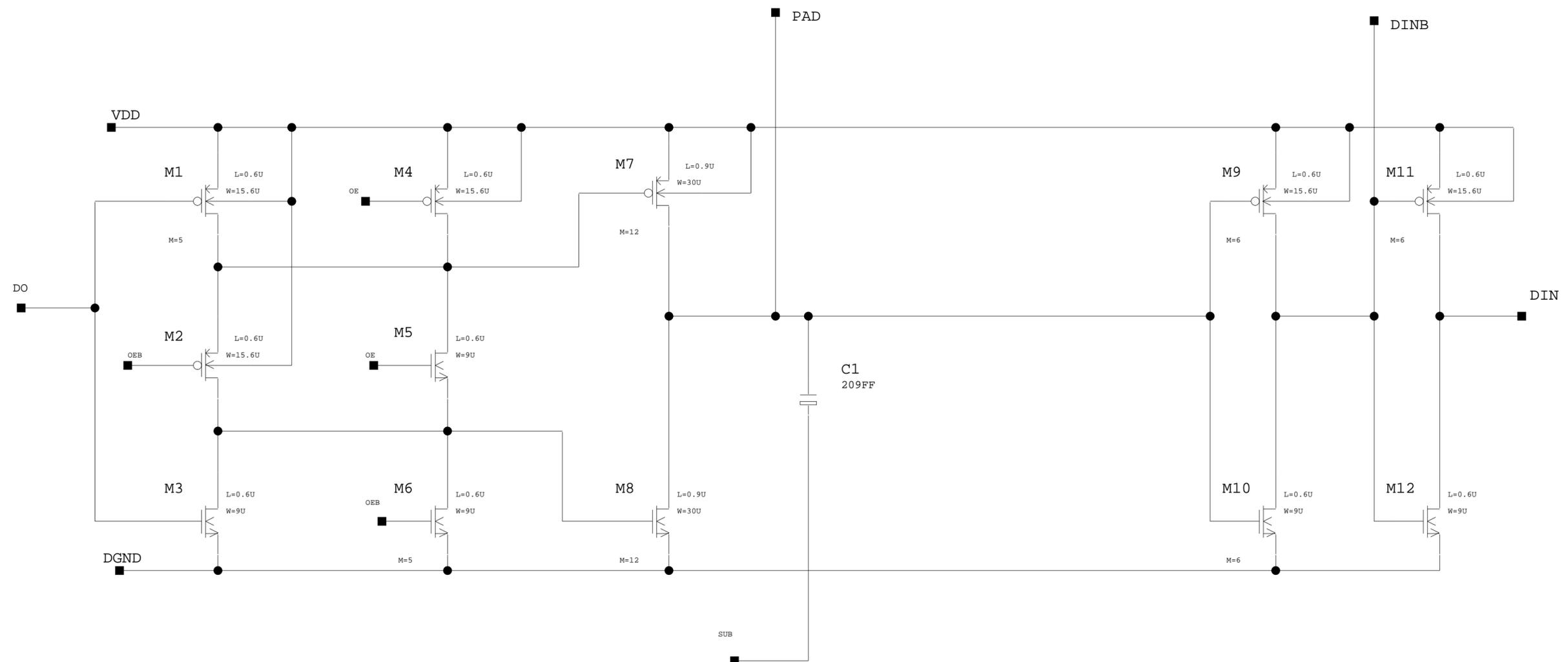
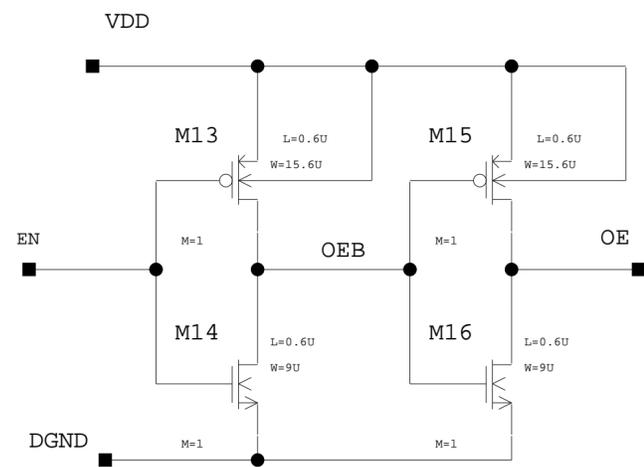
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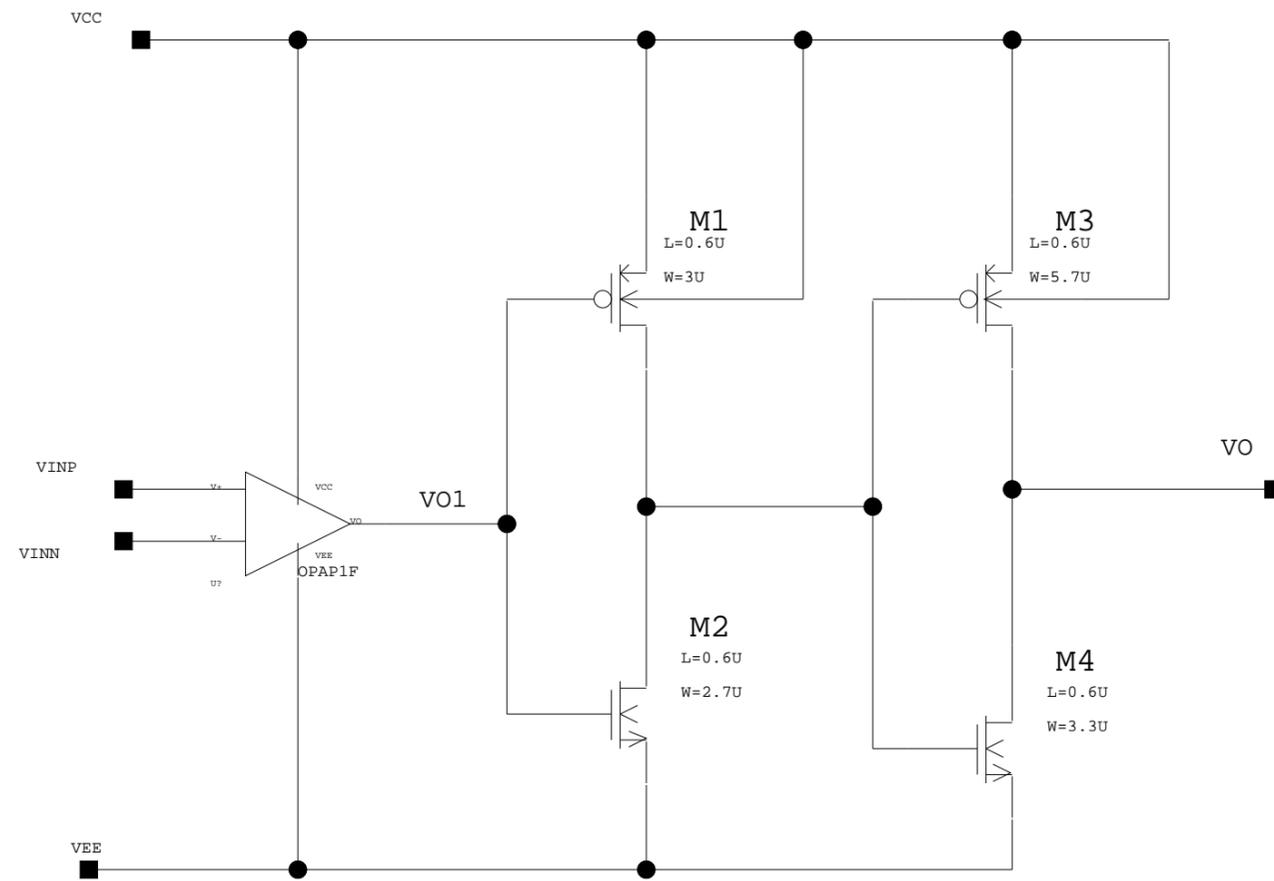
DRAWN BY:

Satpal Singh



11-15-2002_4:15
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10-24-2002_16:20
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VIEWlogic™

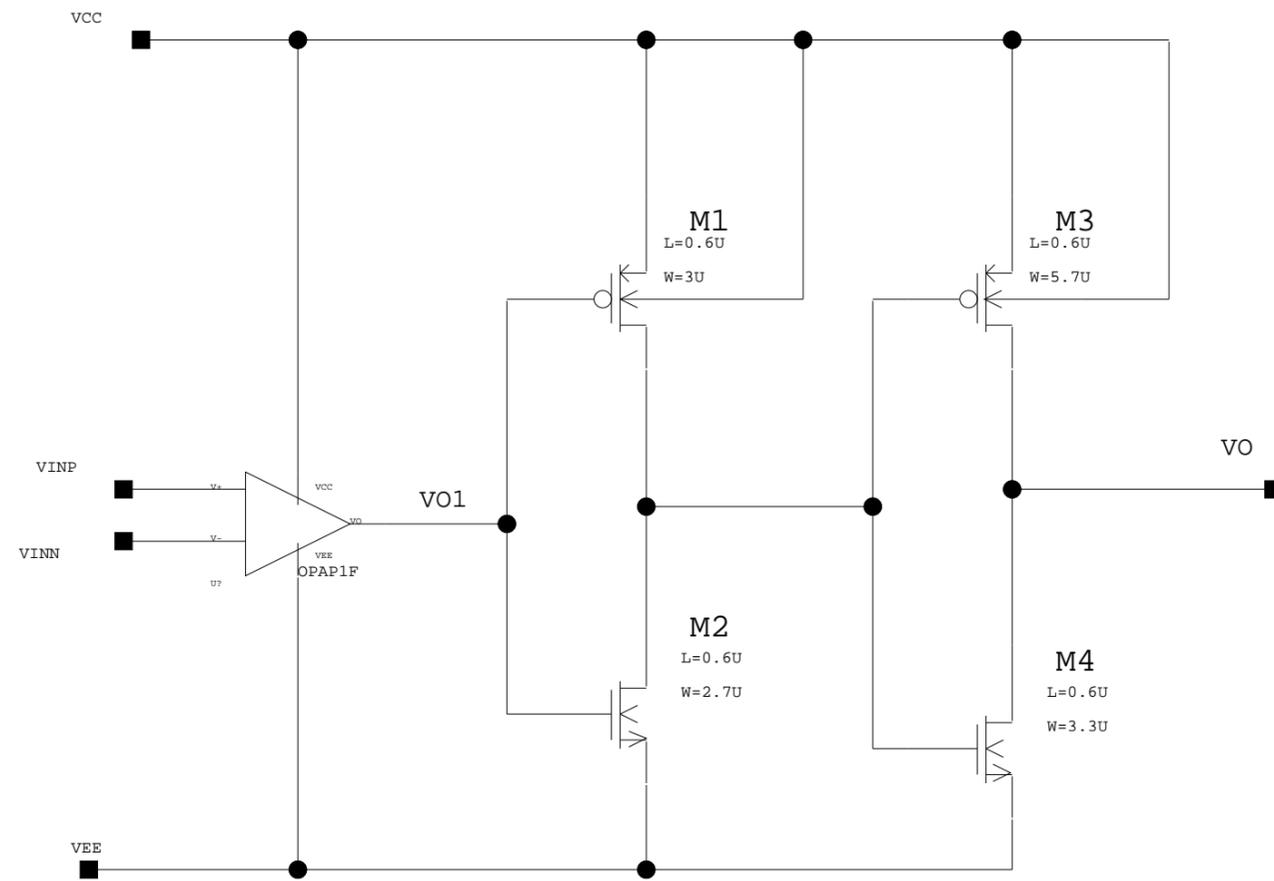
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GLAST / Ag - 0.5u

2.1.02

Ver: GAFE1_1

DRAWN BY: SATPAL SINGH



10-24-2002_16:20

OLVDSRX

VIEWlogic™

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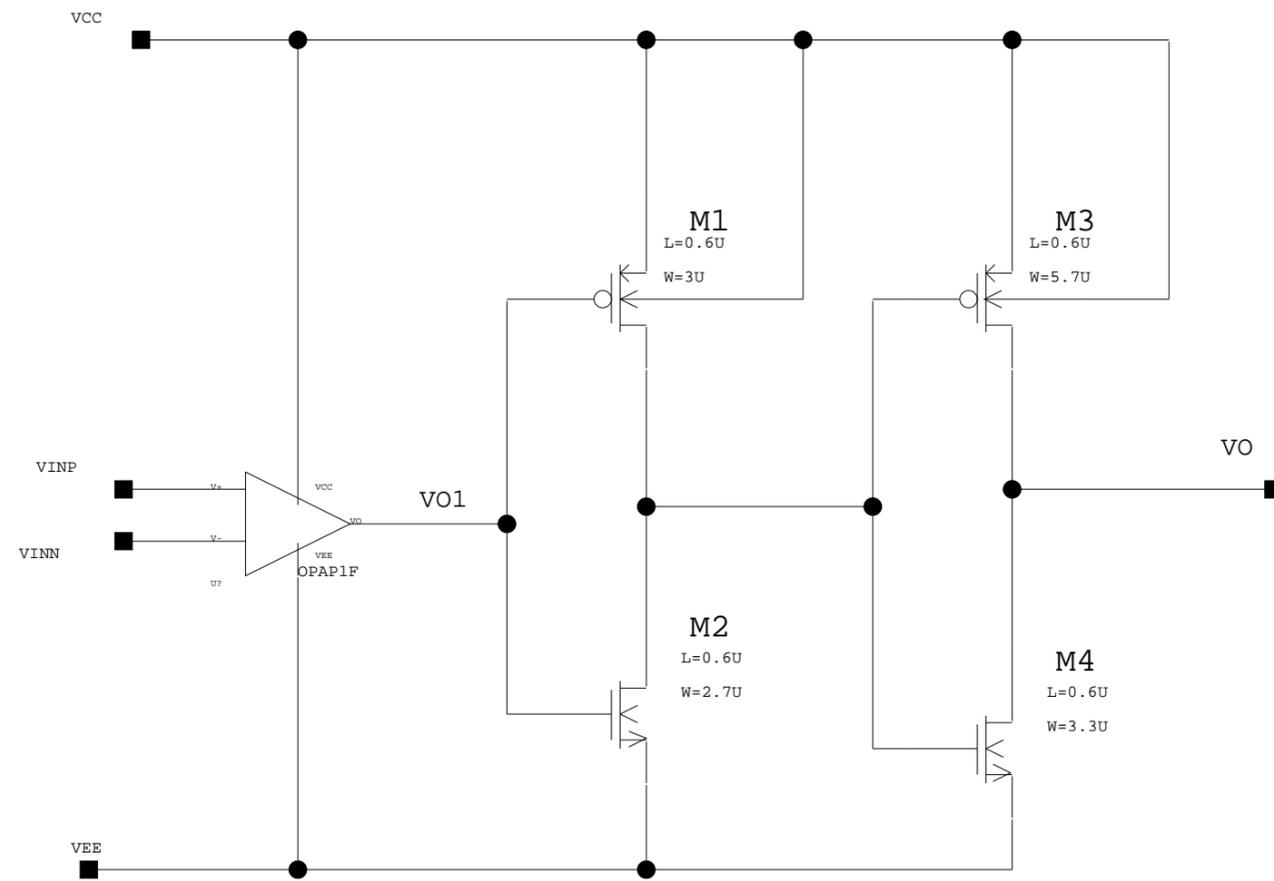
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DRAWN BY:

SATPAL SINGH



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OLVDSRX

VIEWlogic™

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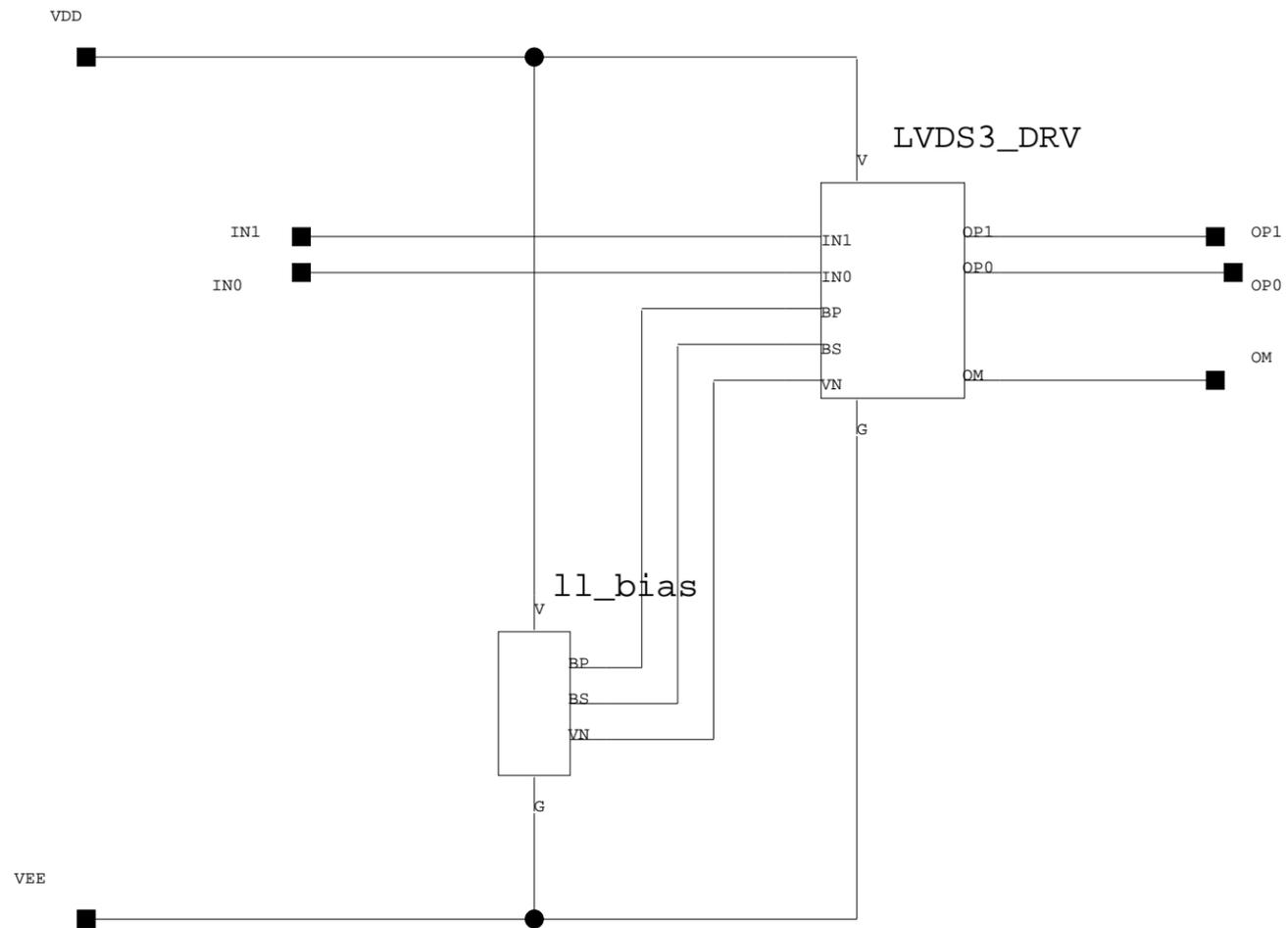
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SATPAL SINGH



9-17-2002_15:10

lvdsdr3

LHEA - NASA

LVDSDR3

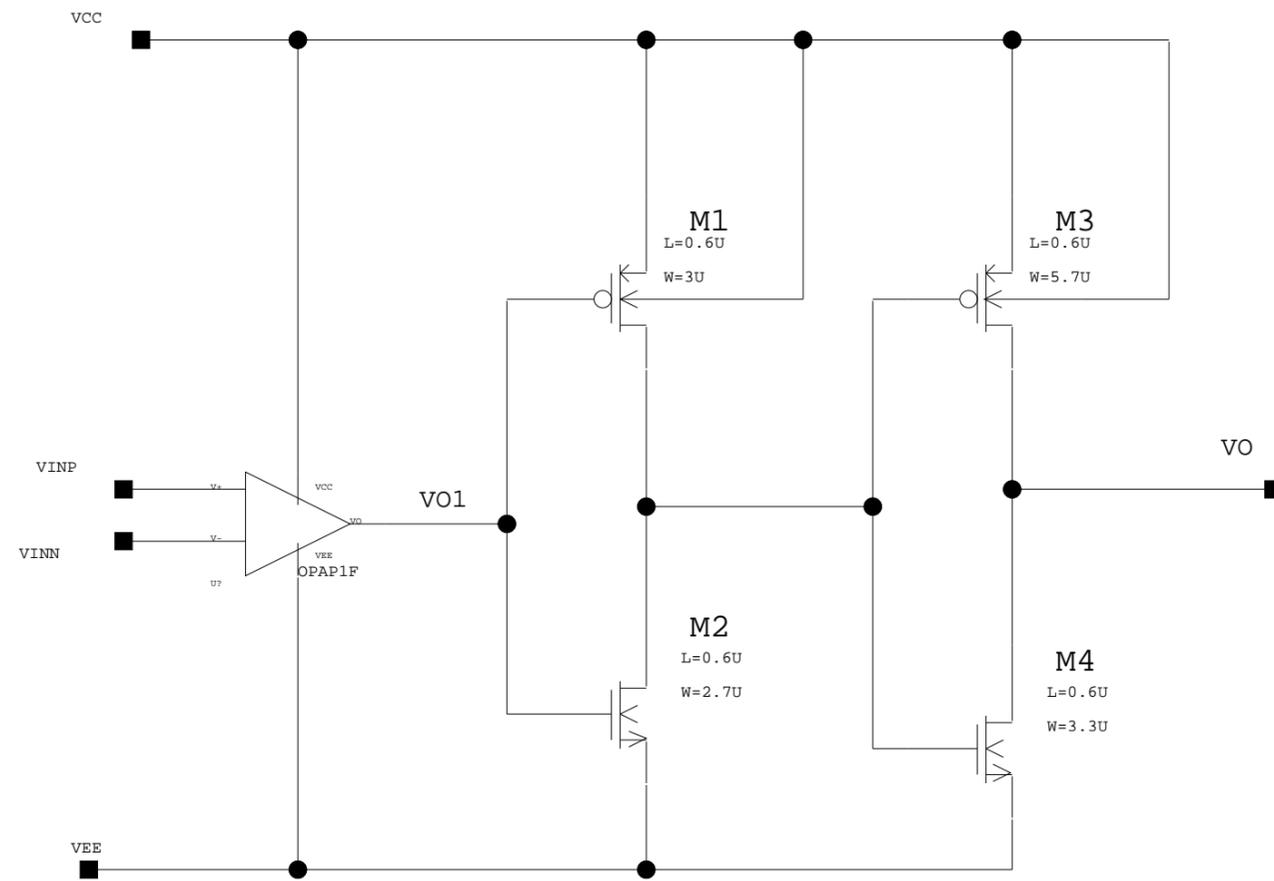
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DRAWN BY:

Satpal Singh



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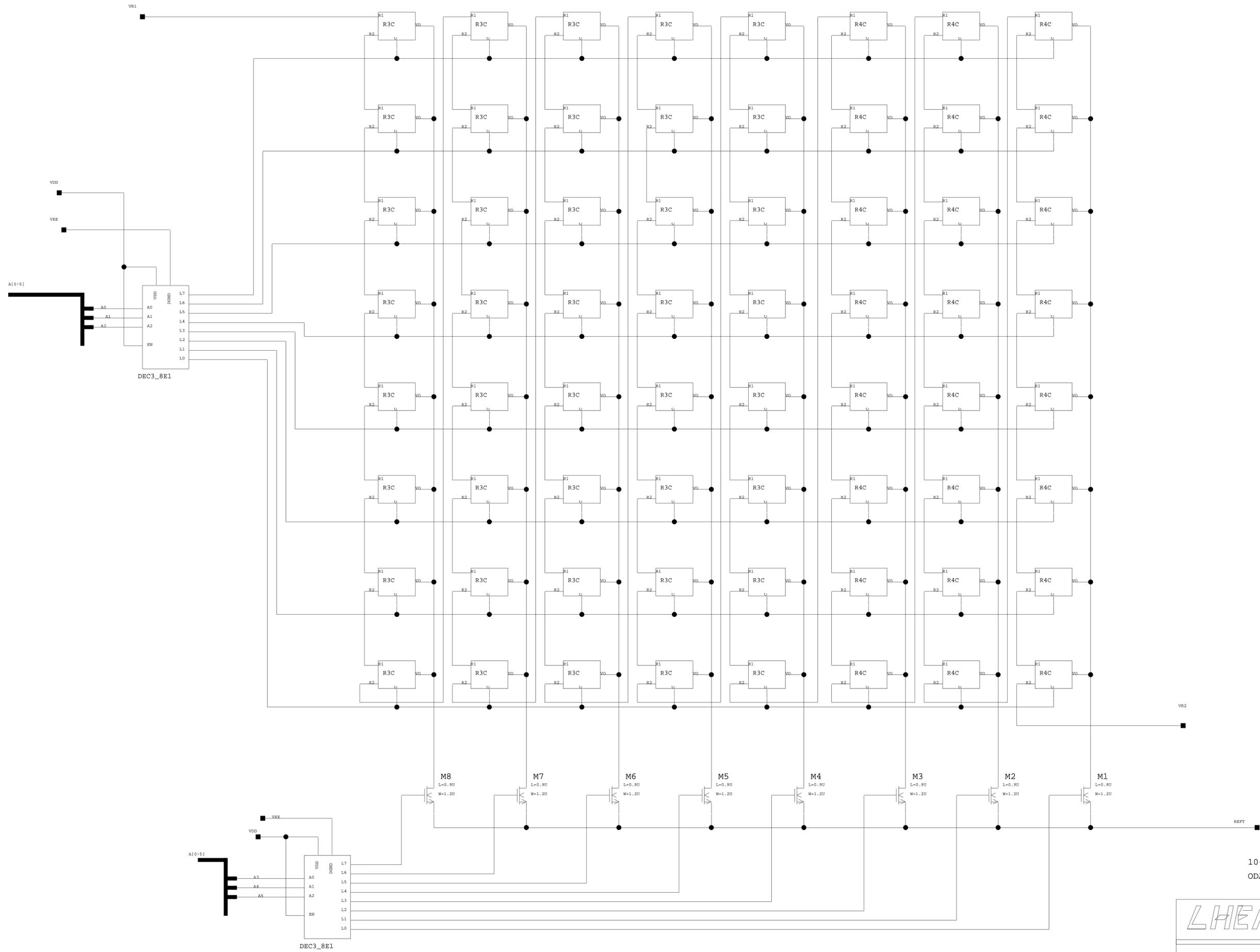
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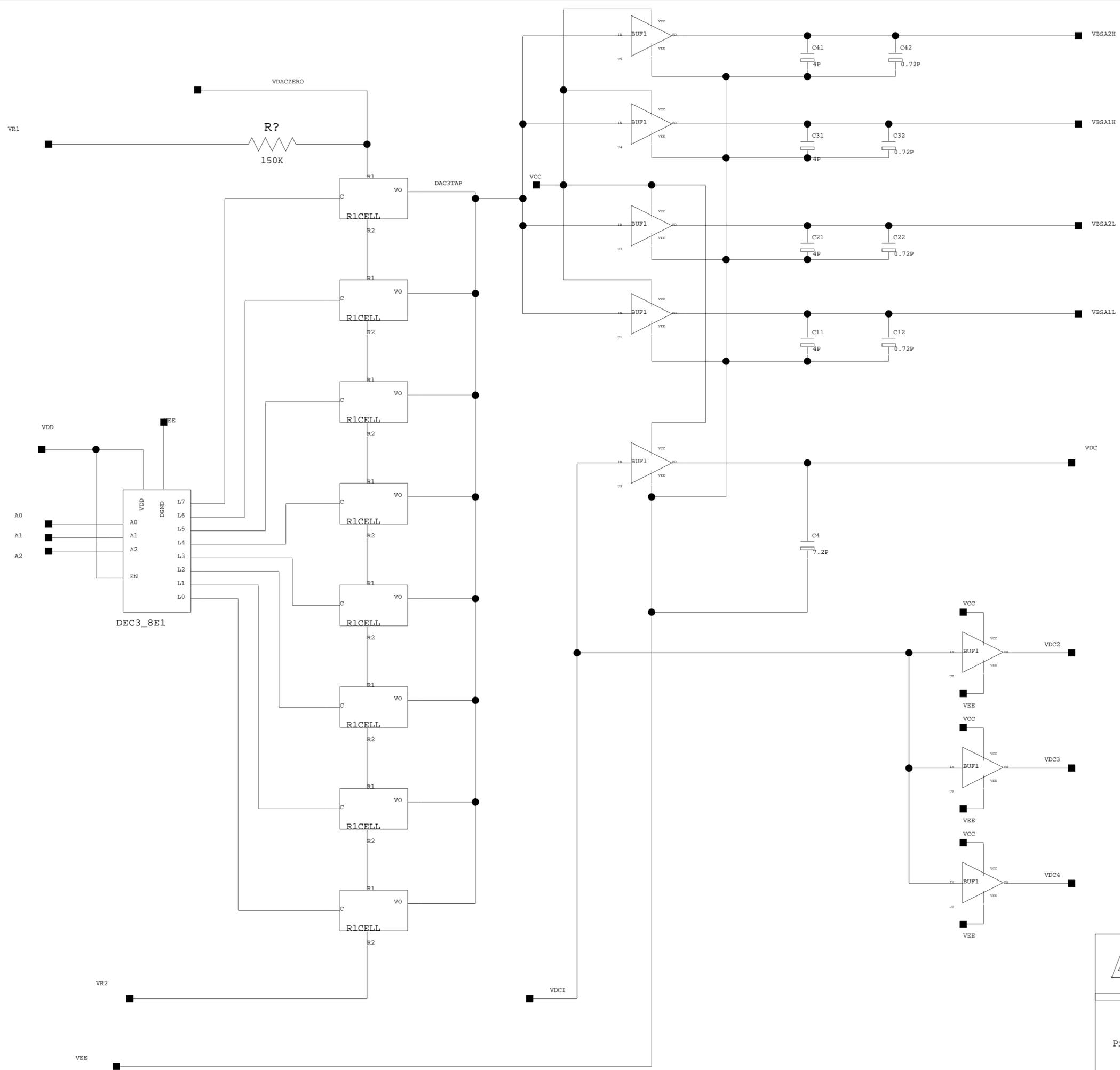


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LHEA - NASA

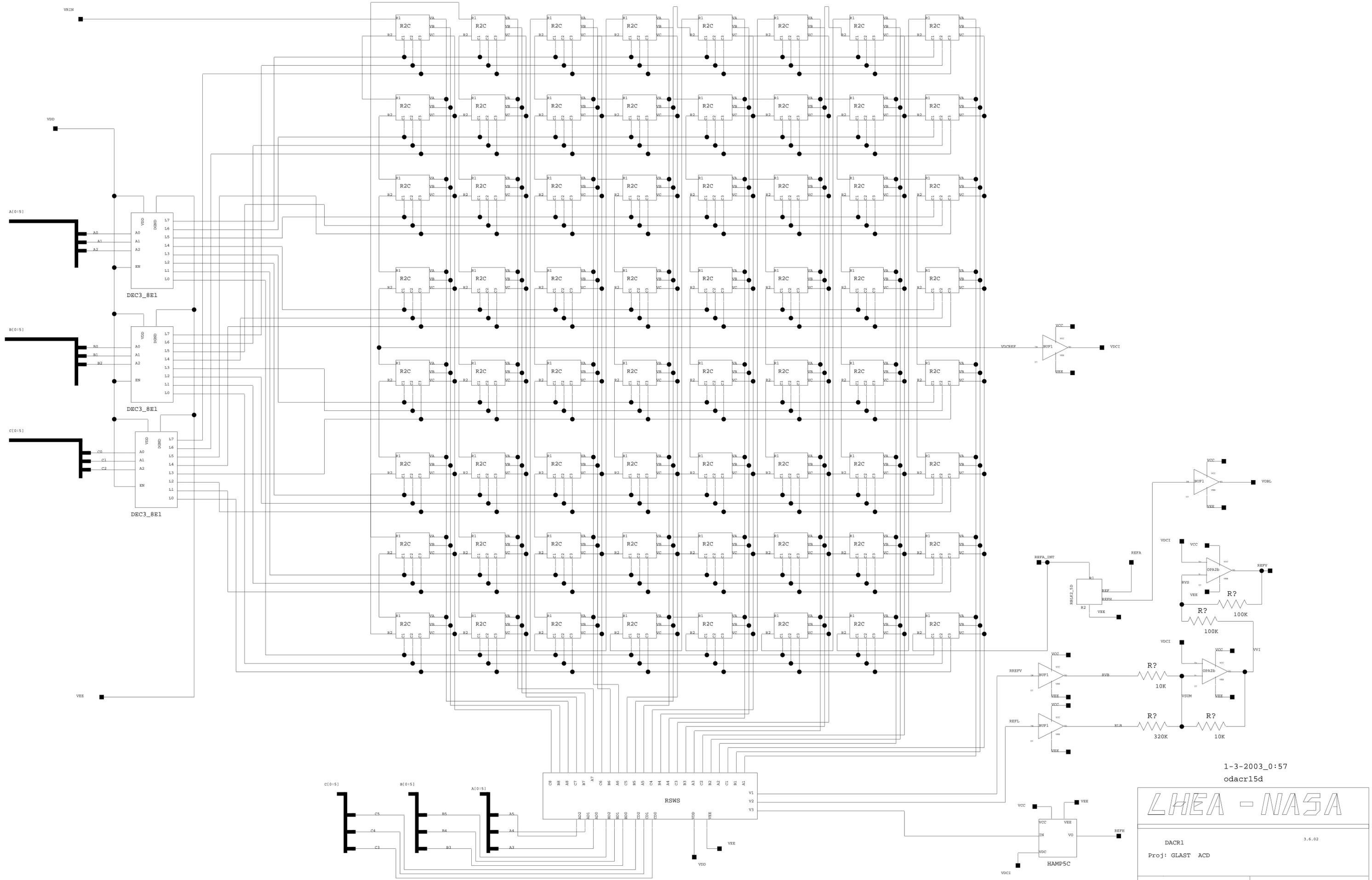
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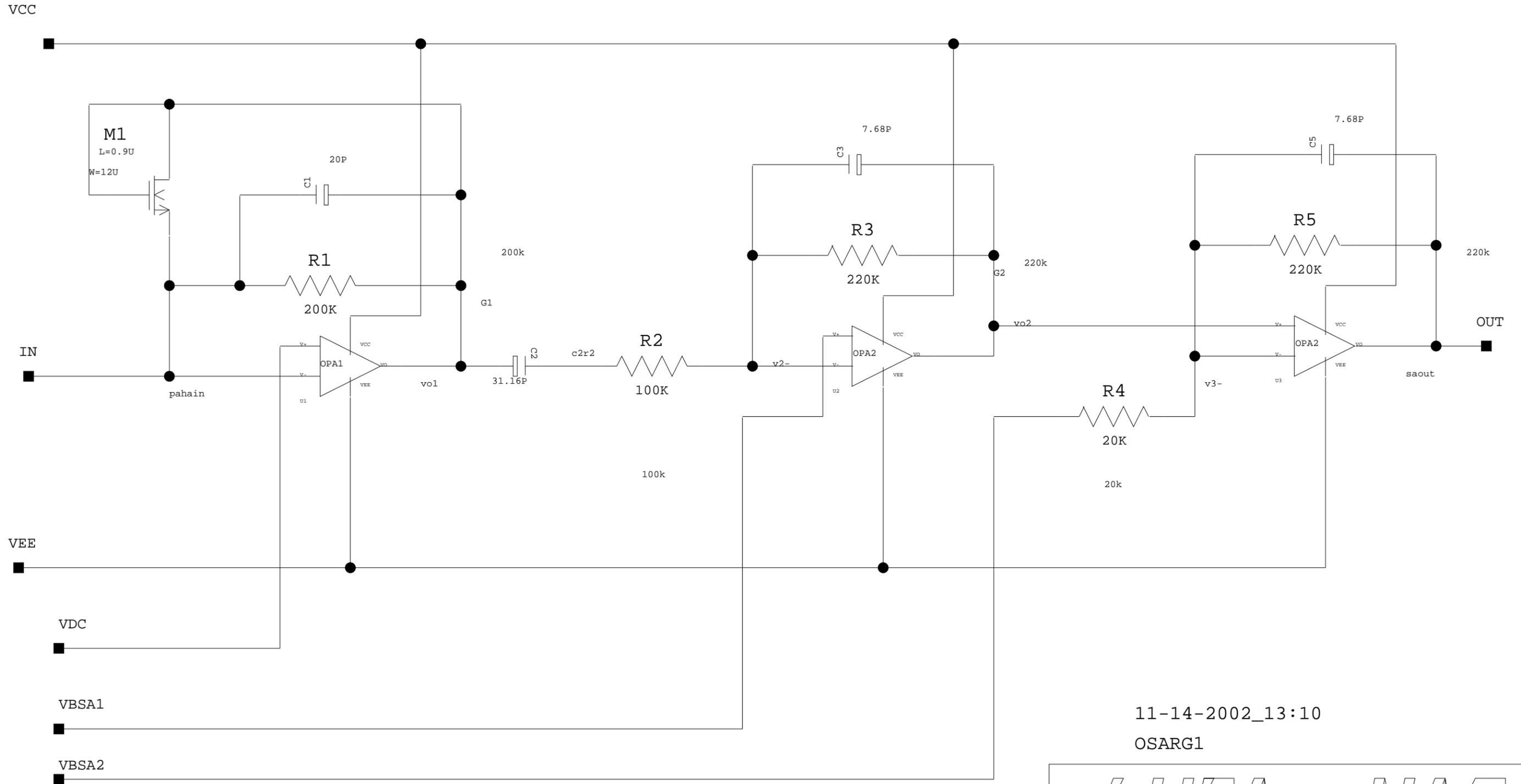
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ver: GAFEL_1	DRAWN BY: Satpal Singh



1-3-2003_0:57
odacr15d



DACR1		3.6.02
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ver: GAF1_1	DRAWN BY:	Satpal Singh



11-14-2002_13:10
OSARG1

LHEA - NASA

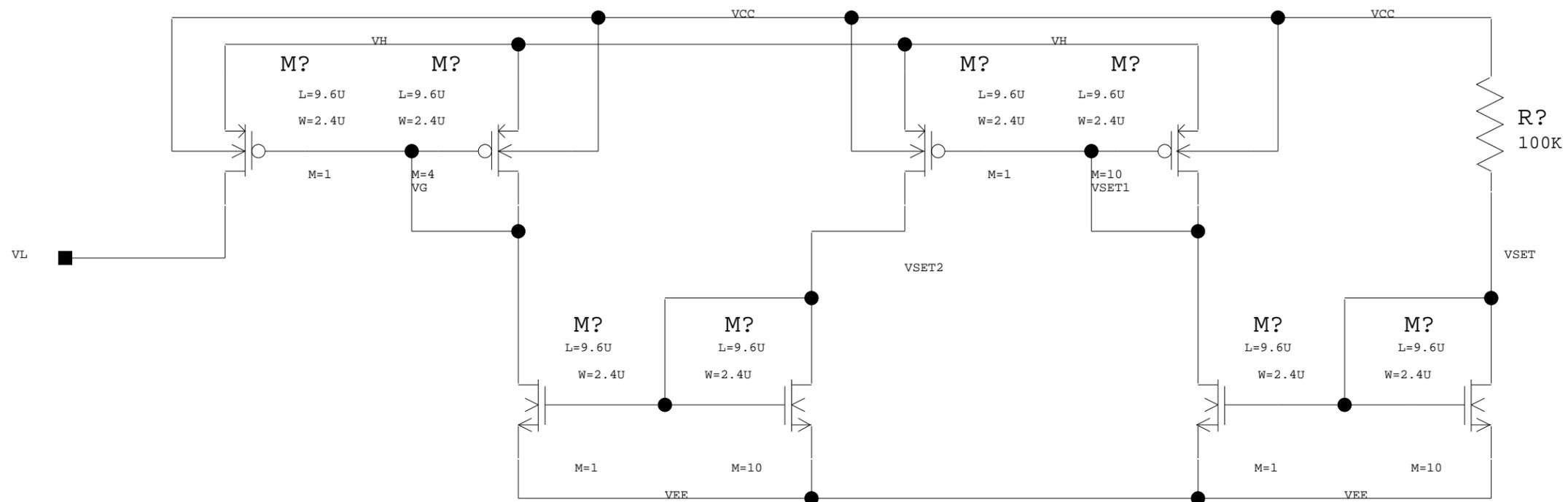
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GLAST ACD

7.18.01

Ver: GAFE1_1

DRAWN BY: SATPAL SINGH

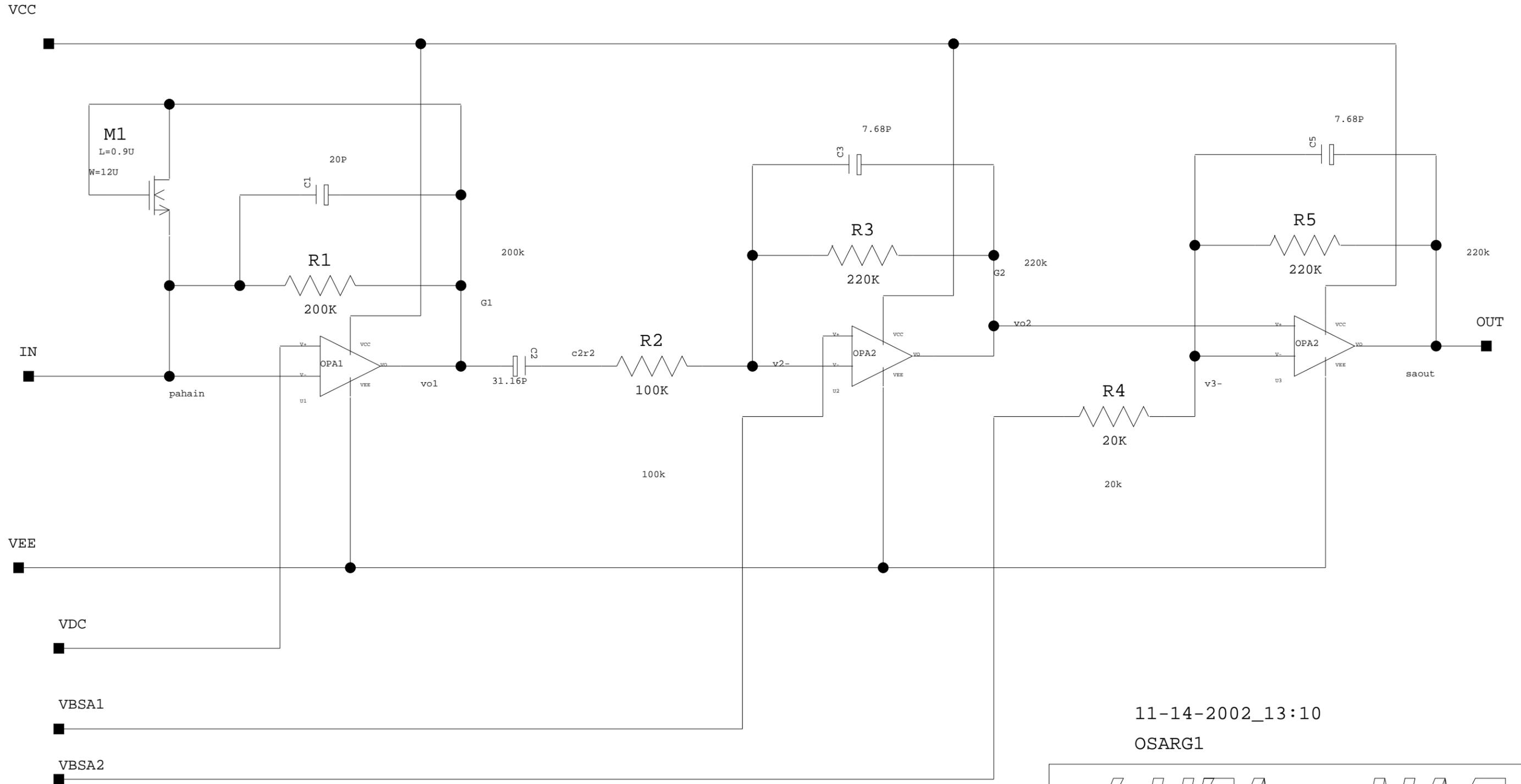


Stanford Linear Accelerator Cent

PRES
adjustable mosfet resistor

OM 22OCT08

DRAWN BY: Oren Milgrome



LHEA - NASA

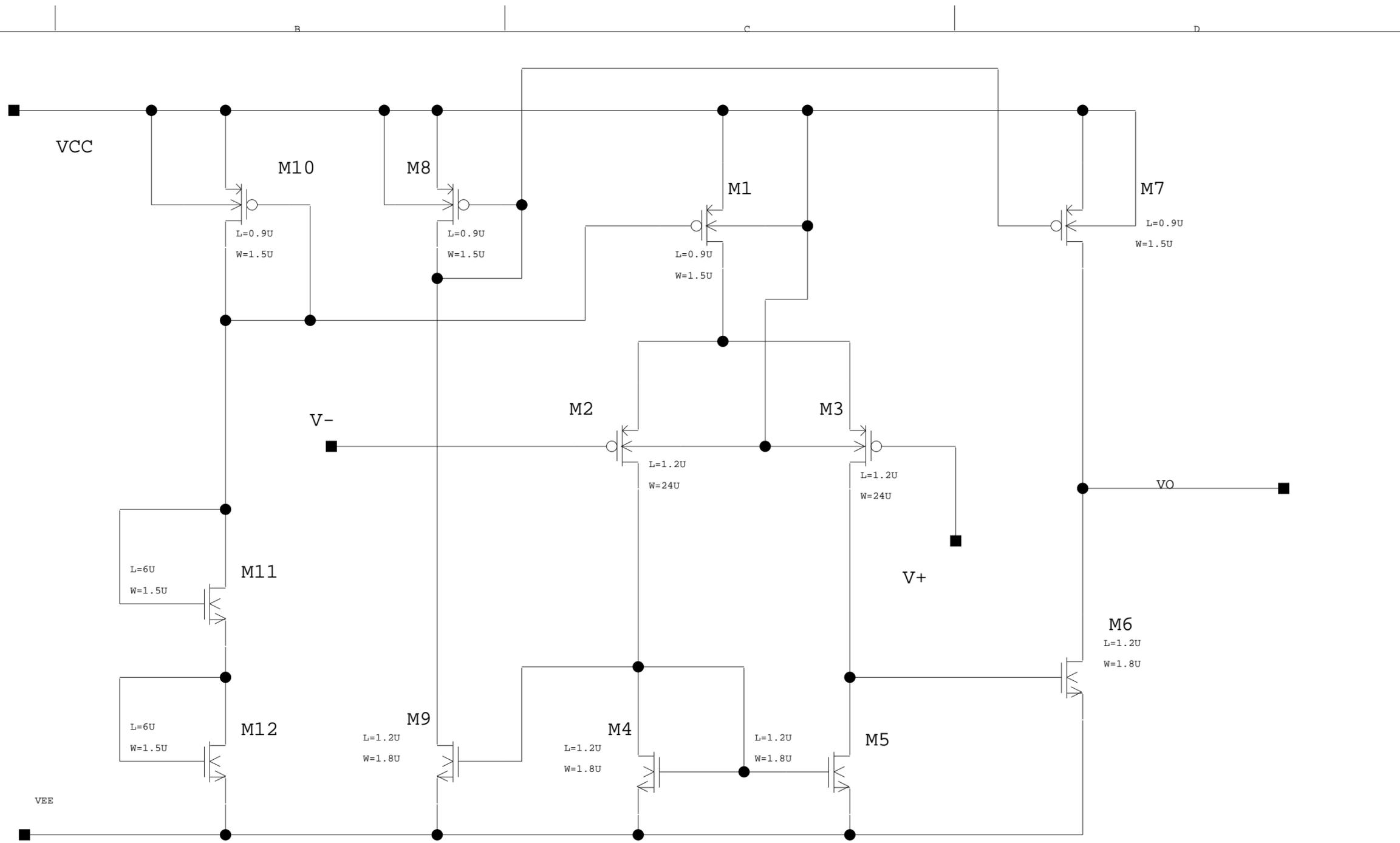
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7.18.01

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DRAWN BY: SATPAL SINGH



10-24-2002_16:19

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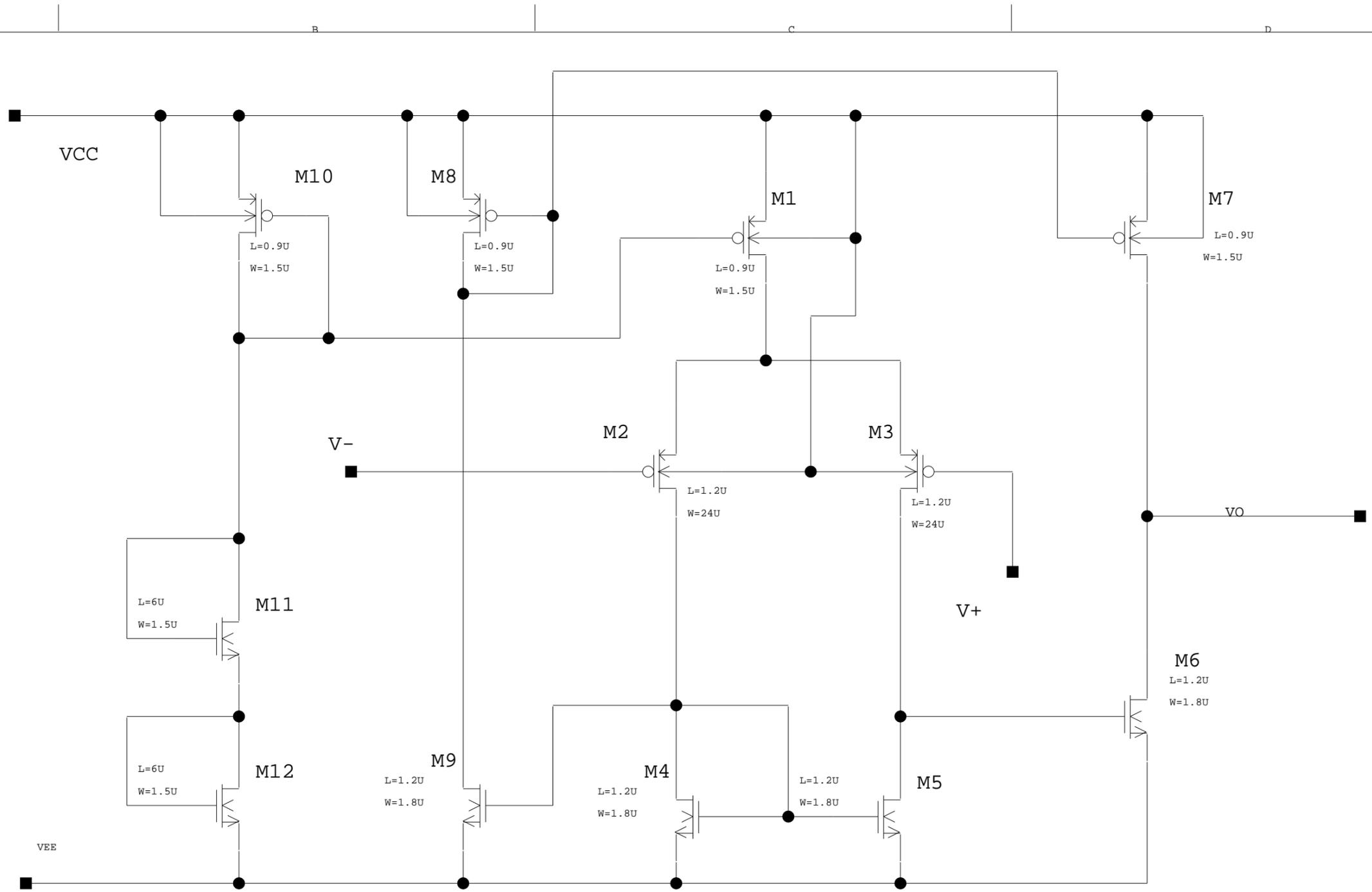
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GLAST ACD

2.1.02

Ver: GAFE1_1

DRAWN BY: SATPAL SINGH



10-24-2002_16:19

OPAP1F

OPAP1F

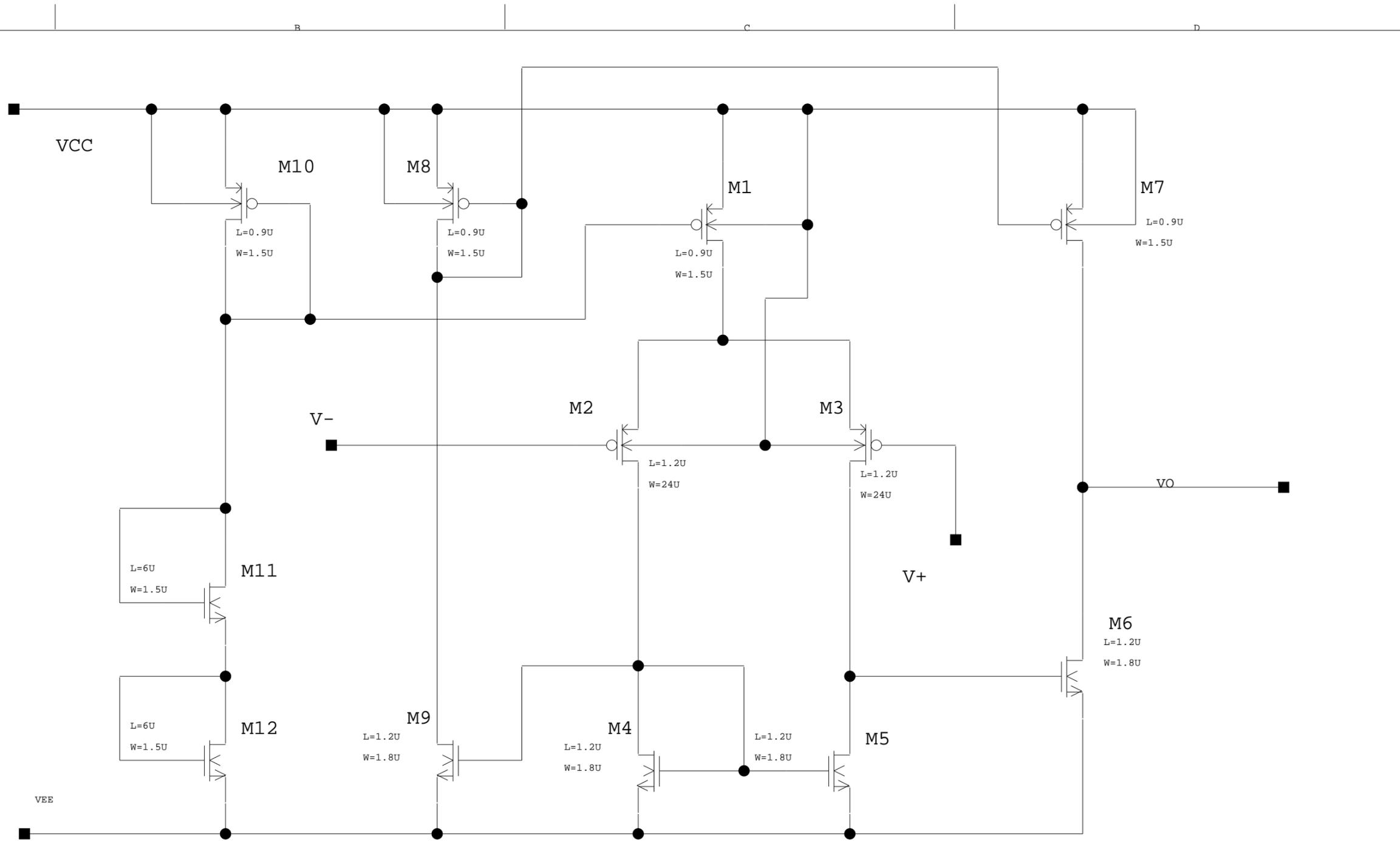
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DRAWN BY:

SATPAL SINGH



10-24-2002_16:19

OPAP1F

OPAP1F

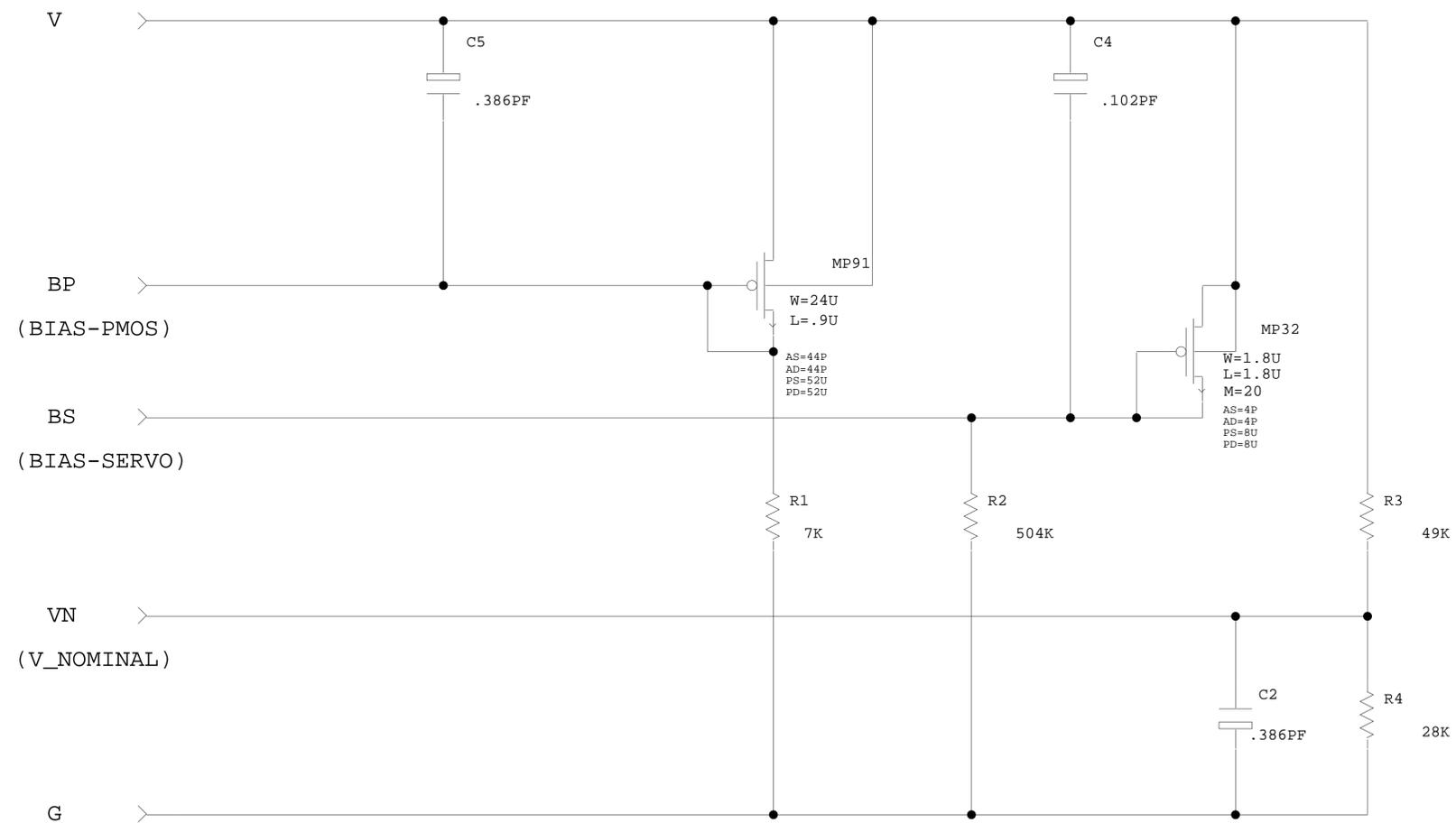
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Ver: GAFE1_1

DRAWN BY:

SATPAL SINGH



1l_bias

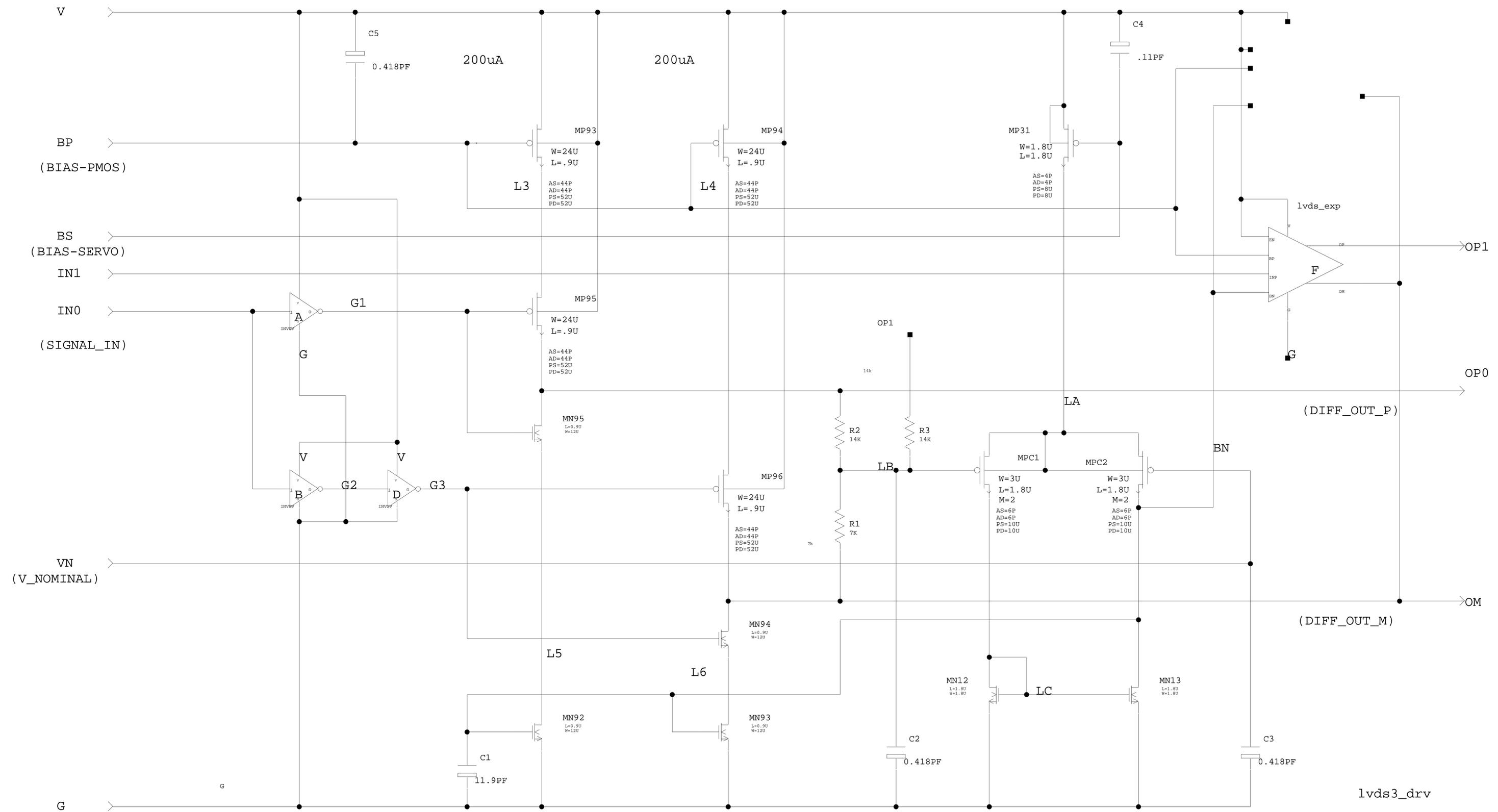
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DFTB		
CHKD		

SHEET		OF

[Empty box]

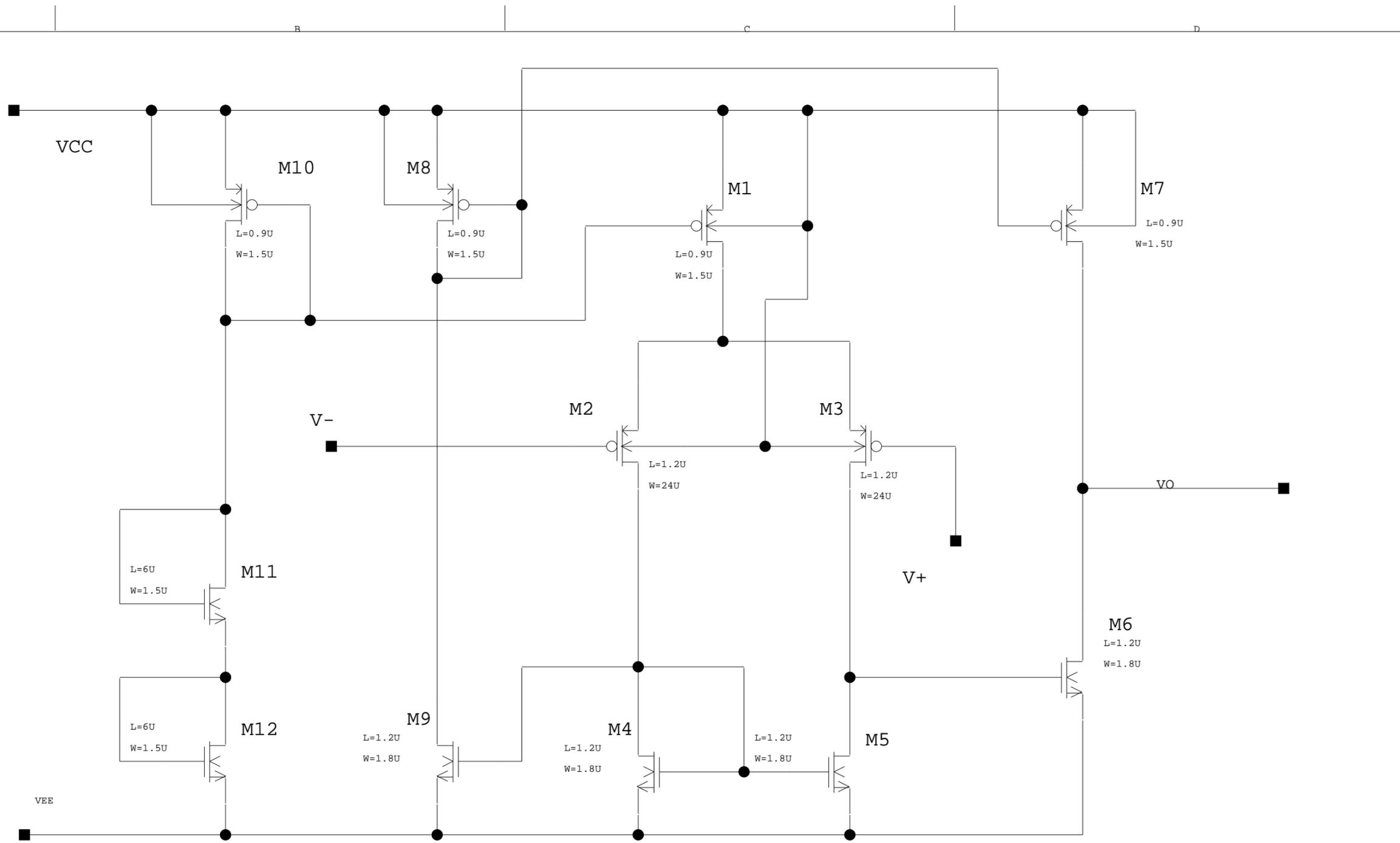
Servo Amplifier



lvds3_drv

9-17-2002_15:10

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ENGR	DATE	APPROVALS
DFTS		
CDRS		



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OPAP1F

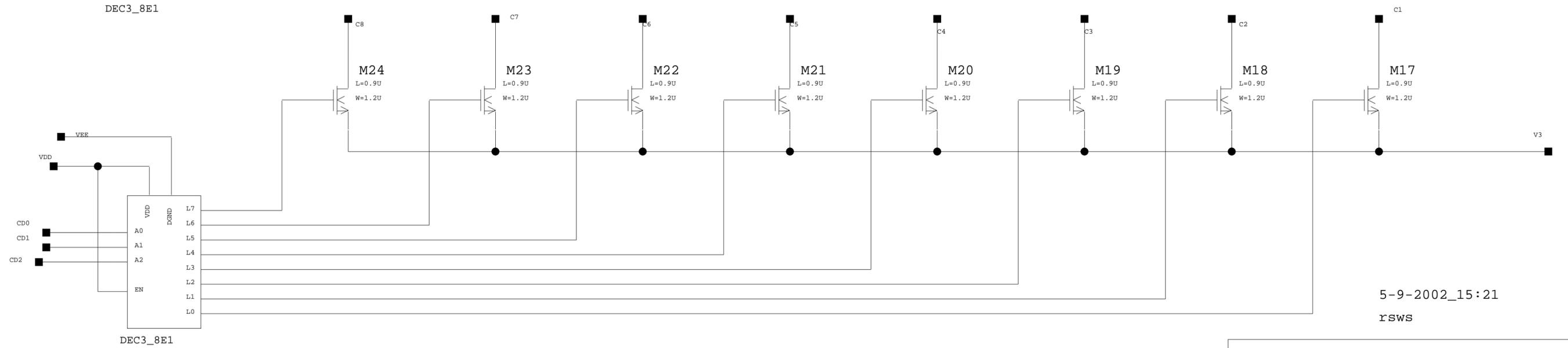
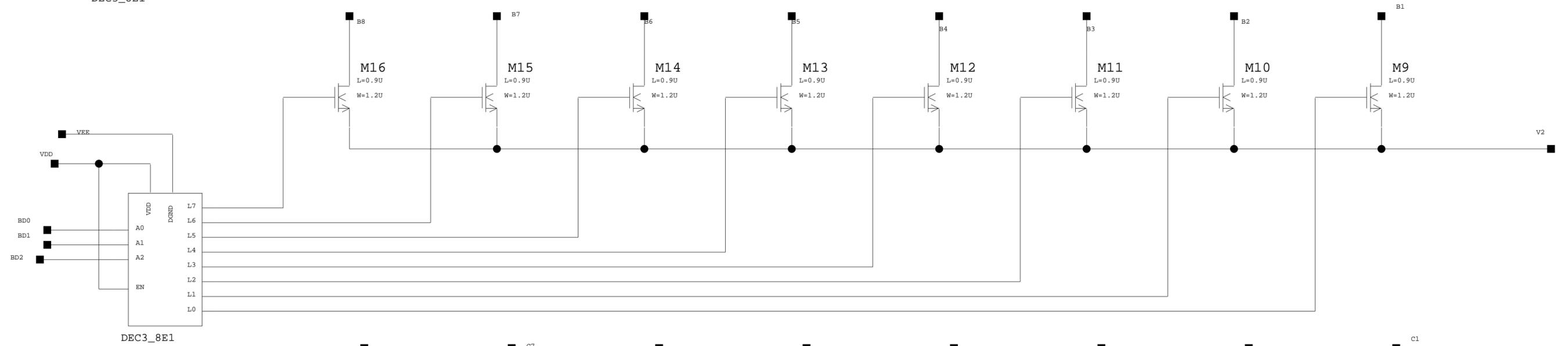
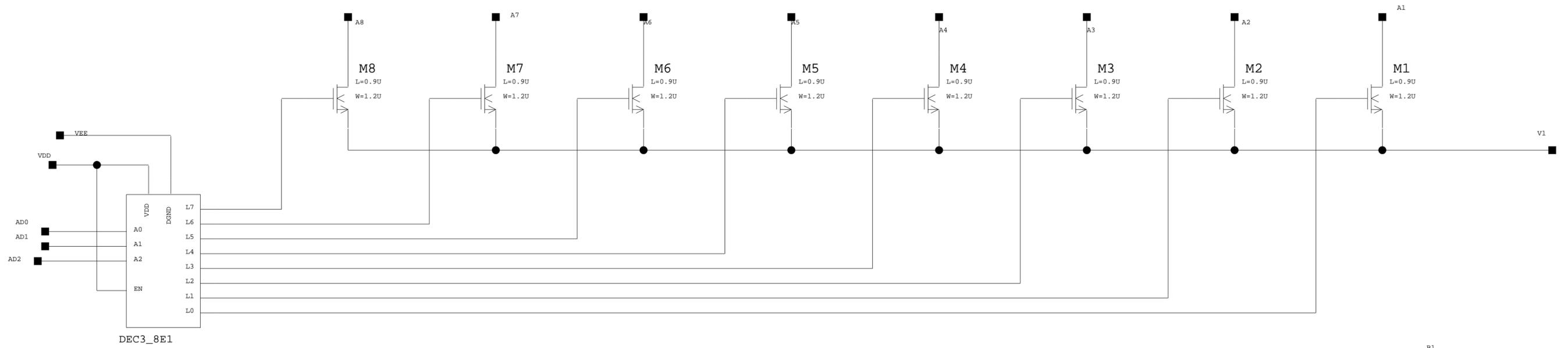
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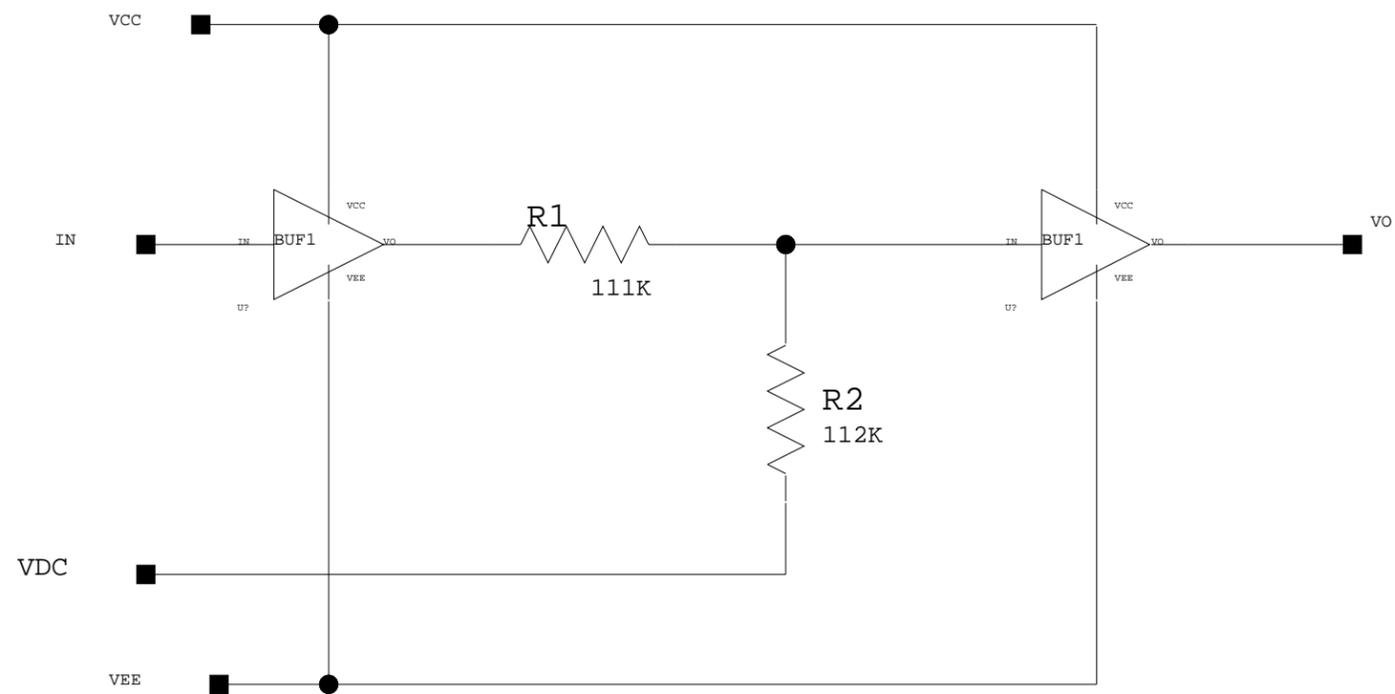
DRAWN BY: SATPAL SINGH



5-9-2002_15:21

RSWS

<h1>LHEA - NASA</h1>	
RSWS	3.6.02
Proj: GLAST ACD	
ver: GAFB1_1	DRAWN BY: Satpal Singh



12-29-2002_15:02

hamp5c

LHEA - NASA

HAMP

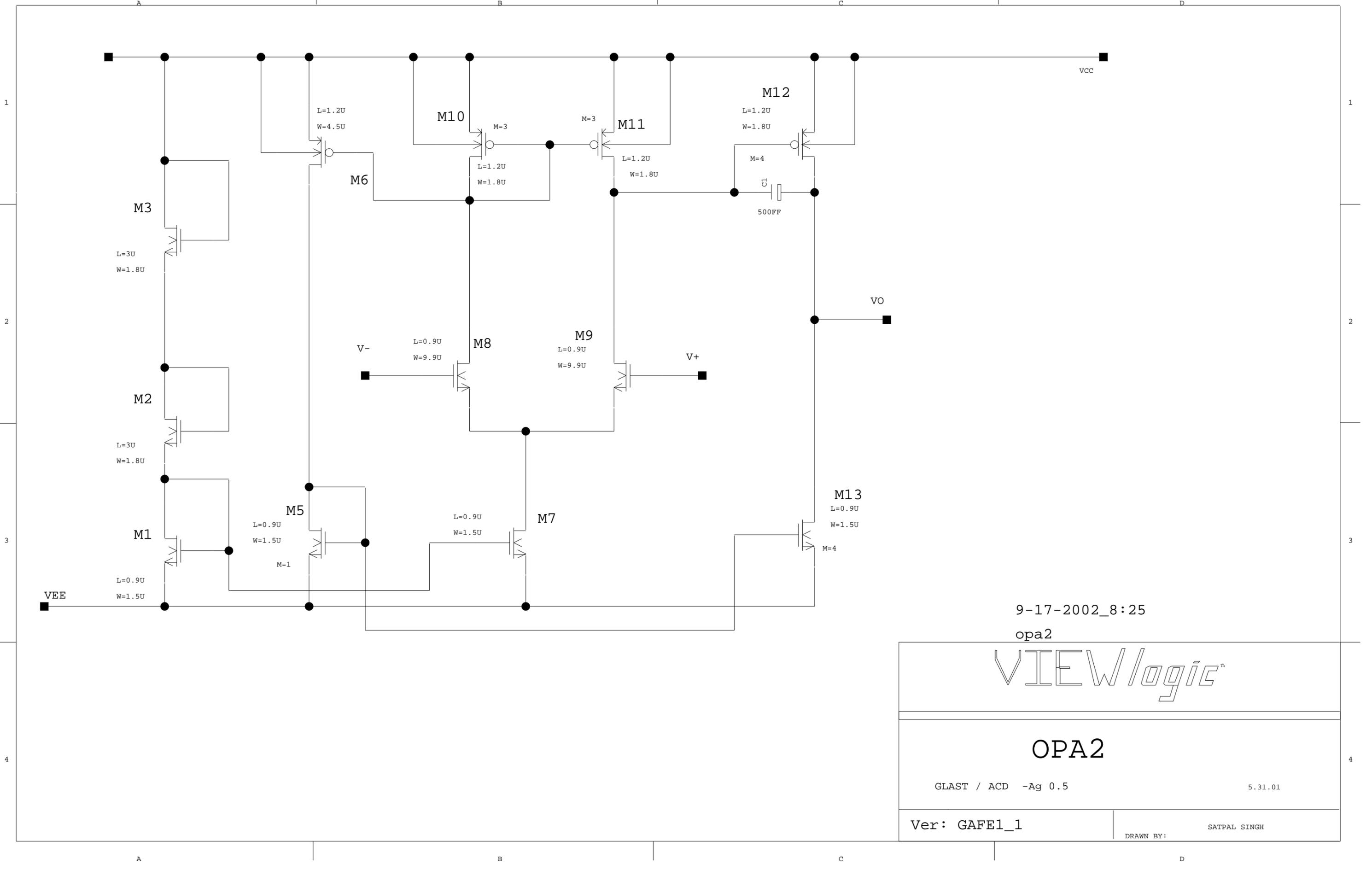
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Proj: GLAST ACD

ver: GAFE1_1

DRAWN BY:

Satpal Singh



9-17-2002_8:25

opa2

VIEWlogic™

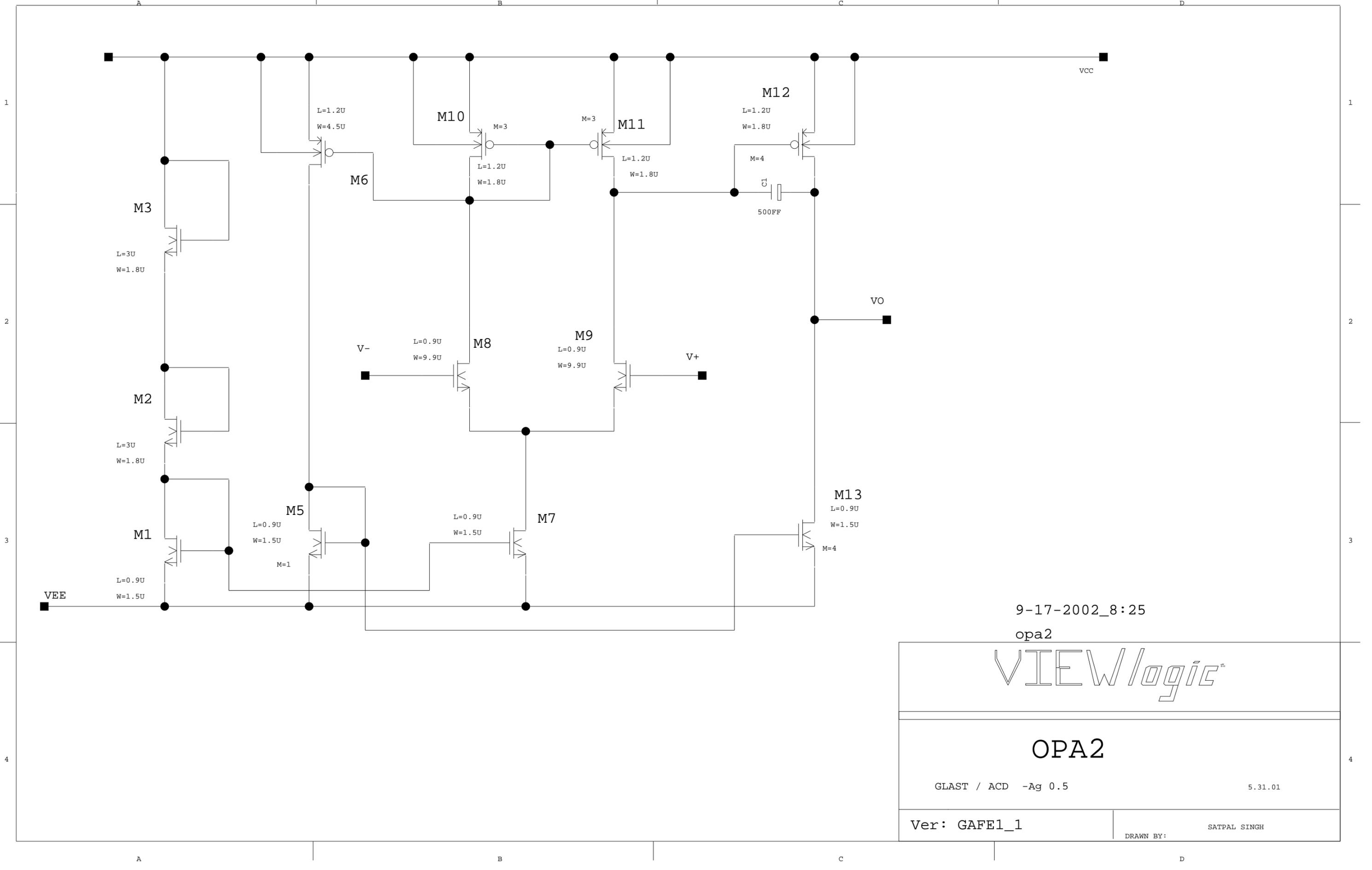
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GLAST / ACD -Ag 0.5

5.31.01

Ver: GAFE1_1

DRAWN BY: SATPAL SINGH



9-17-2002_8:25

opa2

VIEWlogic™

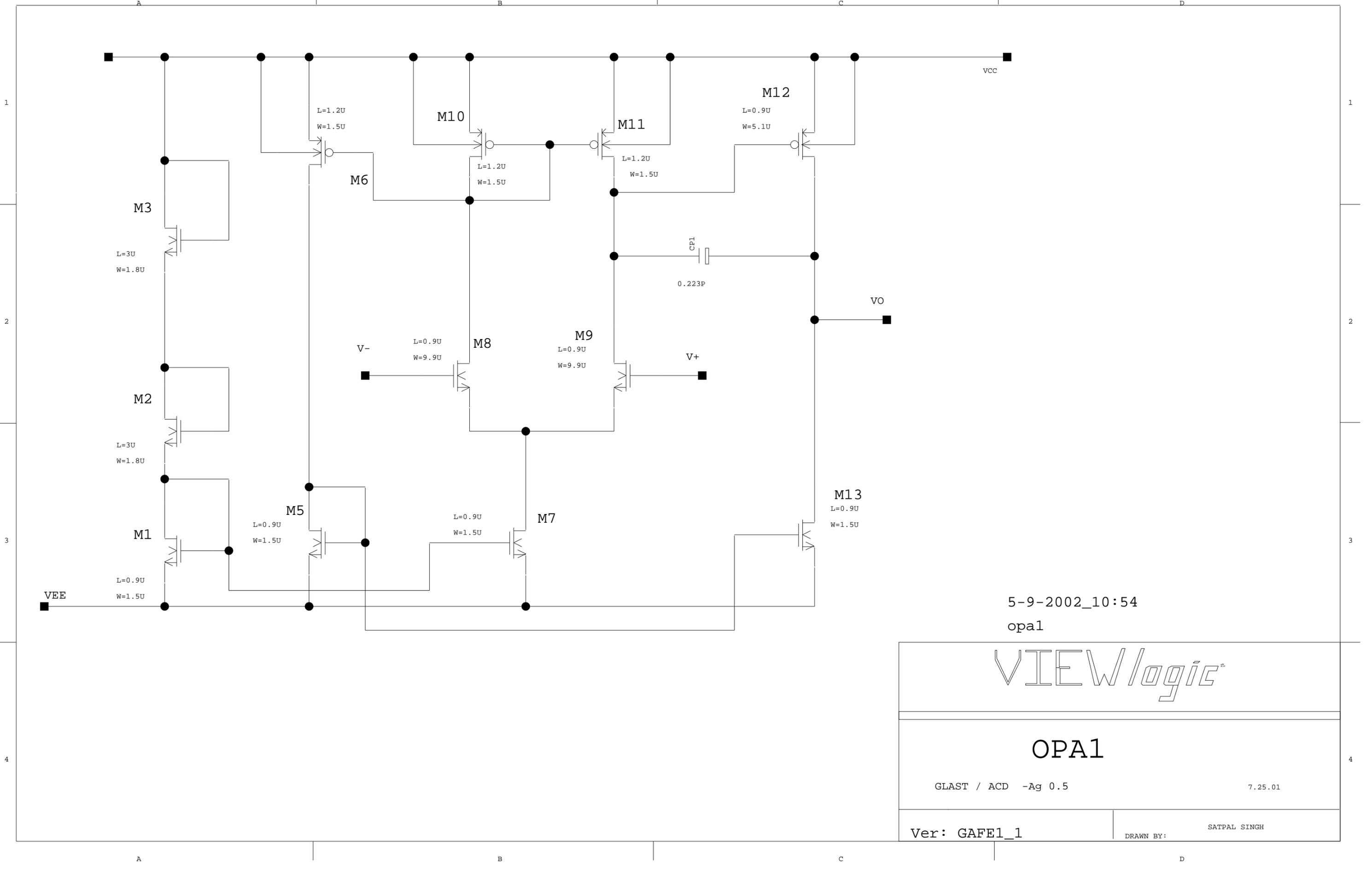
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5.31.01

Ver: GAFE1_1

DRAWN BY: SATPAL SINGH



5-9-2002_10:54
opa1

VIEWlogic™

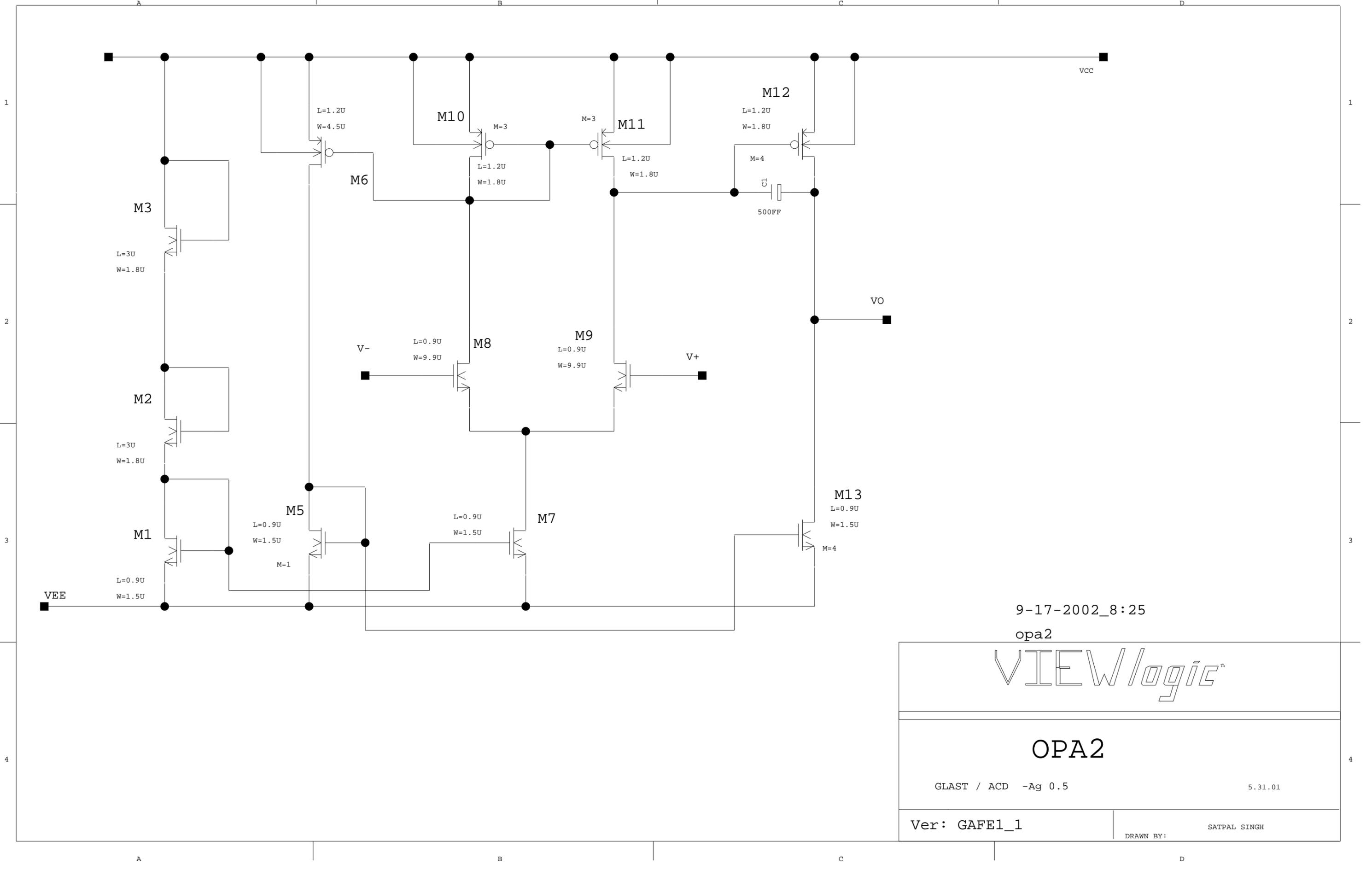
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7.25.01

Ver: GAFE1_1

DRAWN BY: SATPAL SINGH



9-17-2002_8:25

opa2

VIEWlogic™

OPA2

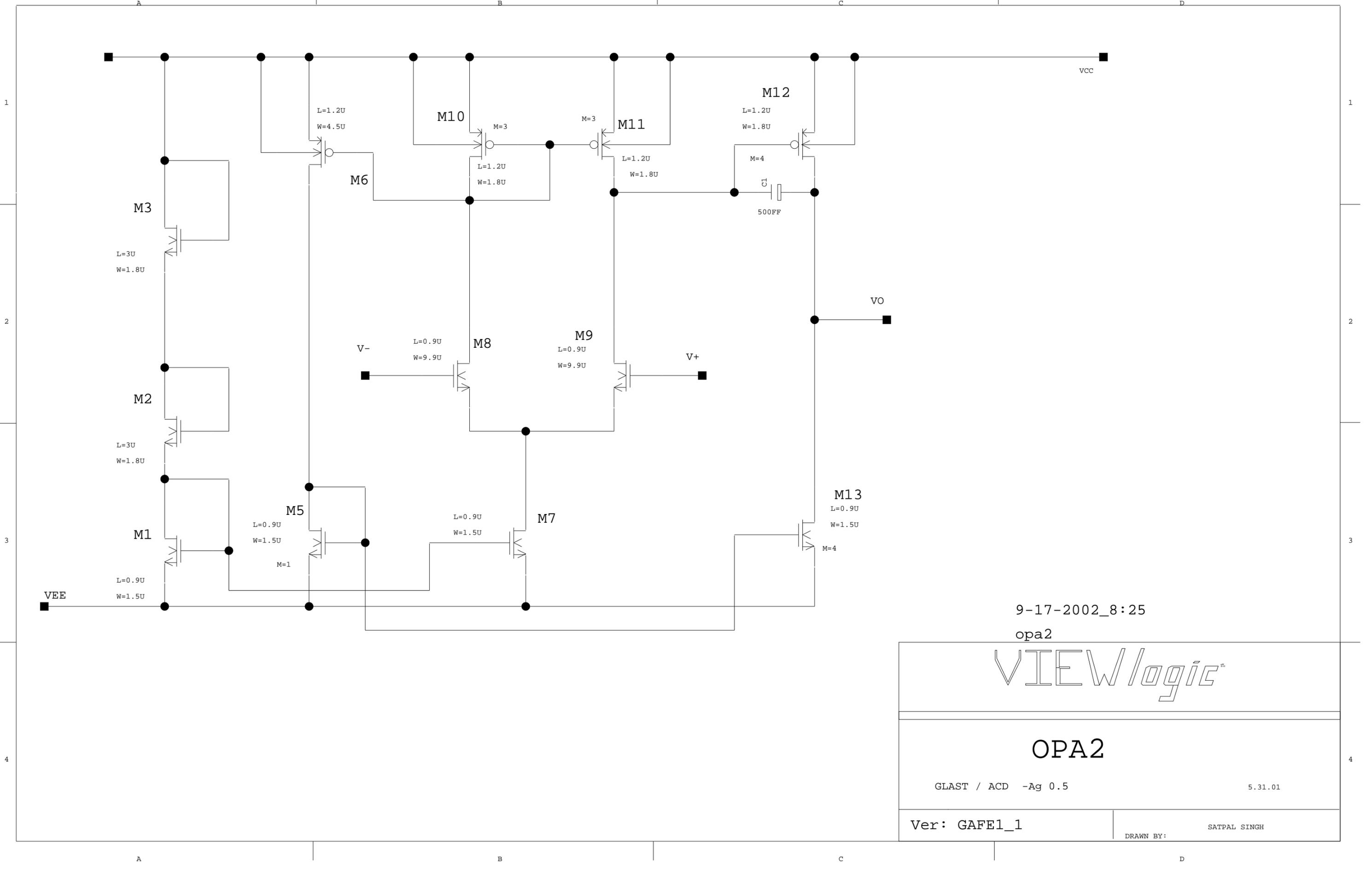
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DRAWN BY:

SATPAL SINGH



9-17-2002_8:25

opa2

VIEWlogic™

OPA2

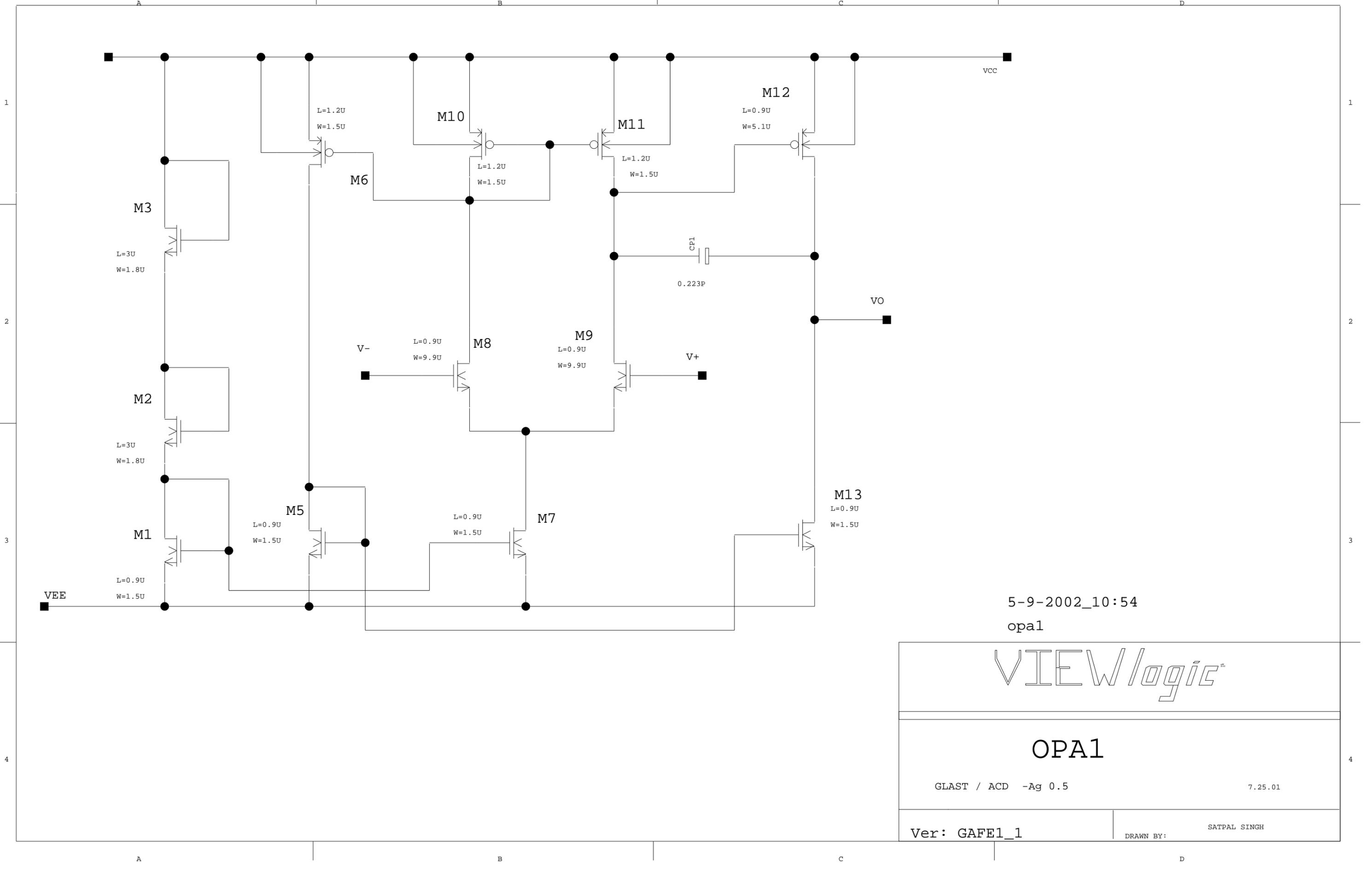
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Ver: GAFE1_1

DRAWN BY:

SATPAL SINGH



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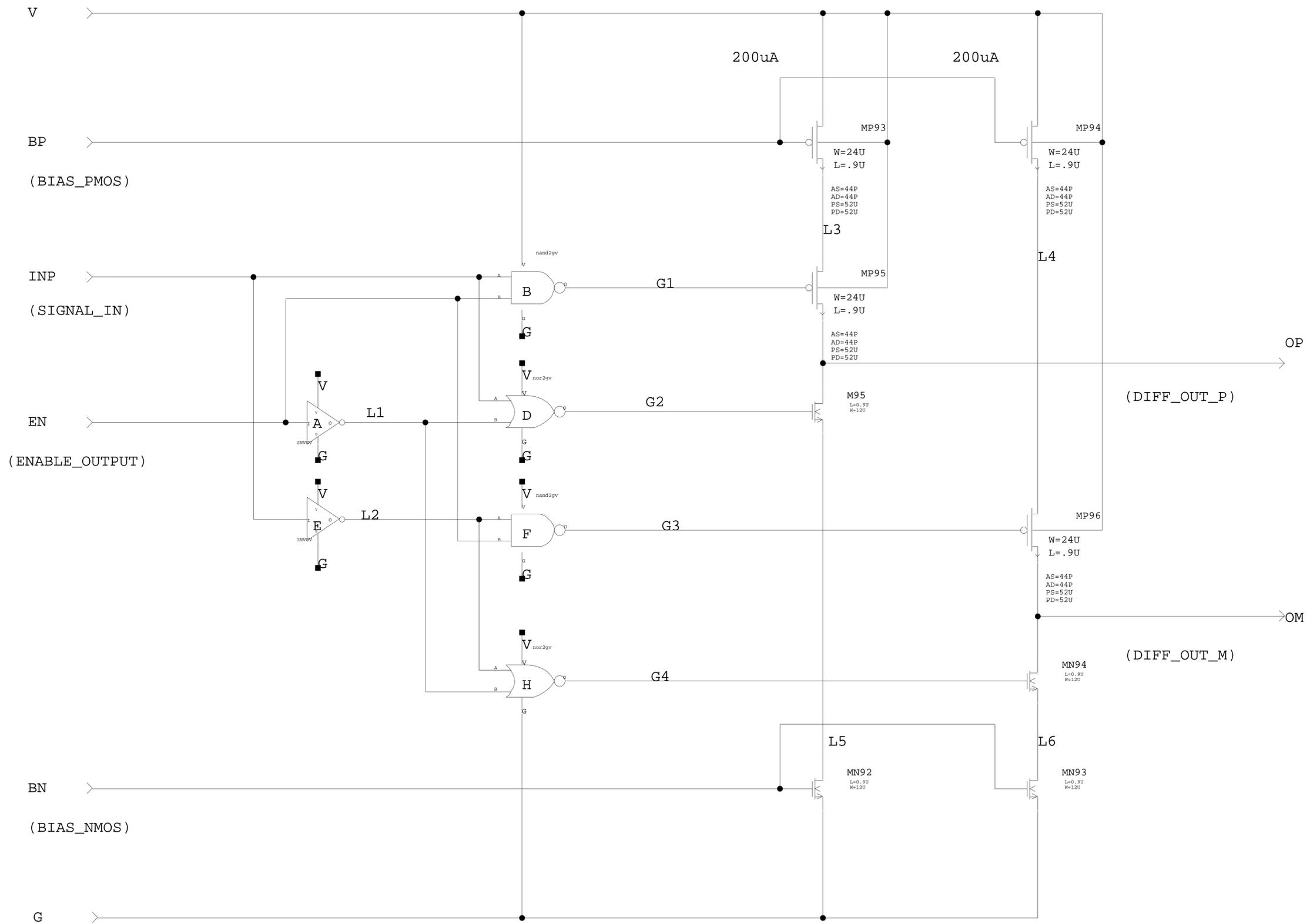
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7.25.01

Ver: GAFE1_1

DRAWN BY: SATPAL SINGH



lvds_exp
5-9-2002_15:29

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